M212758EN-B
RESTRICTED

Hardware Quick Guide

Digital Receiver and Signal Processor

RVP10

VAISALA

PUBLISHED BY

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1. About this document

1.1 Version information

This document provides safety information, a hardware description, and technical specifications for RVP10 Digital Receiver and Signal Processor.

For more information about RVP10, read *RVP10 User Guide (M212604EN)*.

Table 1 Document versions

Document code	Date	Description
M212758EN-B	August 2024	Updated for RVP10 release 2.0.
M212758EN-A	March 2023	First revision.

1.2 Related documents

Table 2 Vaisala Weather Radar documentation

Document code	Name
M213000EN	*Weather Radar WRM200 Installation and Configuration Guide*
M212924EN	*IRIS and RDA Software Installation Guide*
M212925EN	*IRIS and RDA Utilities Guide*
M212926EN	*IRIS Radar User Guide*
M212927EN	*IRIS Programming Guide*
M212928EN	*IRIS Product and Display Guide*
DOC236879	*IRIS RDA Release Notes*
M212604EN	*RVP10 Digital Receiver and Signal Processor User Guide*
M212923EN	*Radar Control Processor RCP8 User Guide*

Vaisala encourages you to send your comments or corrections to helpdesk@vaisala.com.

1.3 Documentation conventions

WARNING! Warning alerts you to a serious hazard. If you do not read and follow instructions carefully at this point, there is a risk of injury or even death.

CAUTION! Caution warns you of a potential hazard. If you do not read and follow instructions carefully at this point, the product could be damaged or important data could be lost.

Highlights important information on using the product.

Gives information for using the product more efficiently.

Lists tools needed to perform the task.

Indicates that you need to take some notes during the task.

1.4 Trademarks

Vaisala® is a registered trademark and IRIS™ and Sigmet™ are trademarks of Vaisala Oyj.

All other product or company names that may be mentioned in this publication are trade names, trademarks, or registered trademarks of their respective owners.

2. Safety

2.1 Safety

WARNING! Turn off to the server computer and disconnect the mains power before installing or removing PCI boards or otherwise opening the server chassis.

WARNING! Never open the IFDR10 unit. Thermal conductive material does not bind properly when unit is reassembled. **Opening IFDR10 voids all warranties.**

CAUTION! Follow local regulations in the installation and usage of the device.

The surface may be hot.

CAUTION! Install IFDR in a suitable enclosure where it is protected from dust and humidity. Ensure the sufficient airflow.

CAUTION! Use ESD protection. See ESD protection (page 8).

CAUTION! Do not modify the unit. Improper modification can damage the product or lead to malfunction.

CLASS 1 LASER PRODUCT
The product includes SFP+ optical transceivers. They are Class 1 Laser Products and comply with US FDA regulations. These products are certified by TÜV and CSA to meet the Class 1 eye safety requirements of EN (IEC) 60825 and the electrical safety requirements of EN (IEC) 60950.
The laser rays are invisible to the human eye.
Even though the optical transceivers are eye-safe, do not look directly into the laser source.

2.1.1 ESD protection

Electrostatic discharge (ESD) can damage electronic circuits. Vaisala products are adequately protected against ESD for their intended use. However, it is possible to damage the product by delivering electrostatic discharges when touching, removing, or inserting any objects in the equipment housing.

To avoid delivering high static voltages to the product:

- Handle ESD-sensitive components on a properly grounded and protected ESD workbench or by grounding yourself to the equipment chassis with a wrist strap and a resistive connection cord.
- If you are unable to take either precaution, touch a conductive part of the equipment chassis with your other hand before touching ESD-sensitive components.
- Hold component boards by the edges and avoid touching component contacts.

3. Hardware description

3.1 Hardware system overview

The major modules supplied with RVP10 are:

- IFDR10 Intermediate Frequency Digital Receiver (IFDR), which is typically mounted inside the radar receiver.
- RVP10SRV server main chassis, which is typically mounted in a 19″ EIA rack (radar cabinet).

RVP10 hardware installation includes mechanical installation and siting, electrical specifications of the interface signals, system-level considerations, and the standard connector panel.

Much of the RVP10 I/O is configured through software. Since there is no custom wiring, internal jumpers, or oscillators, it is easy to insert spare modules.

3.2 IFDR10 hardware

Figure 1 IFDR10

The IFDR10 hardware consists of a printed circuit card assembly contained in a mechanical housing. The tight metal housing gives the device the maximum noise immunity. The housing protects the PCB, a heat sink, and an EMI/RFI barrier. The mounting options are designed to be backwards compatible with RVP901 IFDR. IFDR10 may be mounted flat or upright on either of its side.

The dimensions of the module are 246 mm × 136 mm × 52.5 mm (10.6 in × 5.6 in × 2.0 in)

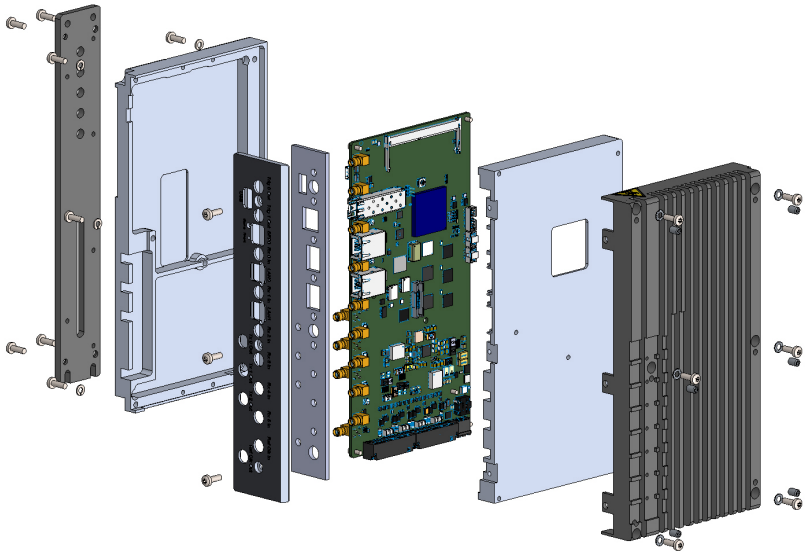

Figure 2 IFDR10 components

3.2.1 Hardware security

IFDR10 has been hardened against unprivileged access and execution of malicious software in the device. Firmware integrity is verified in all stages of code execution by checking the firmware signatures before execution. This permits only official signed firmware by the device manufacturer to execute.

Any attempt to use modified firmware in the IFDR10 will lead to a signature verification failure, making the IFDR10 hardware unusable. IFDR10 does not contain any predefined login credentials or passwords, which prevents any unauthorized access into the embedded Linux operating system running the device. The only access into the IFDR10 settings and configuration are via the interfaces Vaisala provides.

3.2.2 IFDR10 connectors

Figure 3 IFDR10 front connector panel

Table 3 IFDR10 front connector panel

Label	Type	Description
Trig 0 Out	SMA	General purpose trigger I/O
Trig 1 Out	SMA	General purpose trigger I/O
SFP 0	SFP+	10 Gbps fiber optic network link
Rx 0 In	SMA	Direct IF input functionally assigned with `ifd_settings`
LAN 0	RJ-45	1 Gbps Ethernet
Rx 1 in	SMA	Direct IF input functionally assigned with `ifd_settings`
LAN1	RJ-45	1 Gbps Ethernet
Rx 2 in	SMA	Direct IF input functionally assigned with `ifd_settings`
Rx 3 in	SMA	Direct IF input functionally assigned with `ifd_settings`
Rx 4 in	SMA	Direct IF input functionally assigned with `ifd_settings`
Rx 5 in	SMA	Direct IF input functionally assigned with `ifd_settings`
Ref Clk in	SMA	Reference clock input
USB	USB-C	Used for manufacturing purposes. Currently no field applications.
Tx 0 out	SMA	Direct Transmit IF output
Tx 1 out	SMA	Direct Transmit IF output
Tx 2 out	SMA	Direct Transmit IF output
Ref Clk out	SMA	Reference clock output

Label	Type	Description
Status	LED indicator light	Reserved for future development
Reset	Switch	Tactile, momentary on switch. Returns the IFDR10 IP Address and FPGA image to factory boot defaults.

The GPIO connector panel consist of 8 independent I/O stages, which can be flexibly configured as one differential input or output, or two single-ended input or output. Differential interface is implemented using a standard half-duplex RS485 transceiver. Both differential transmitter and receiver are independently controlled. In the single-ended mode, both differential transmitter and receiver are disabled. The input/output and single-ended/differential modes are set for pin pairs (GPIO0 and GPIO1, GPIO2 and GPIO3, and so on). Setting pins of the same pin pair to different modes is not possible.

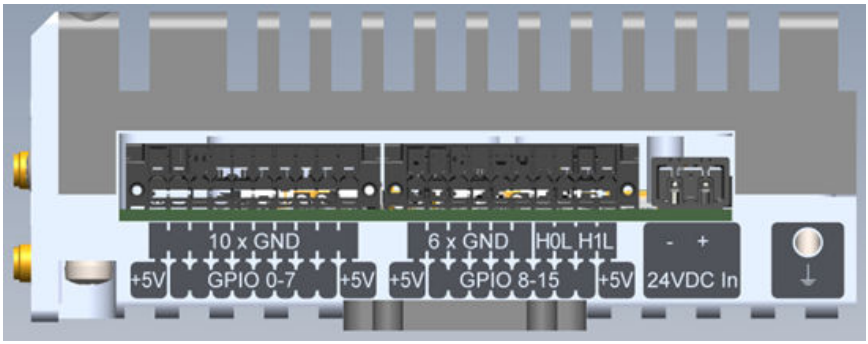

Figure 4 IFDR10 GPIO connector panel

Table 4 Electrical properties of GPIO pins in single-ended mode

Parameter	Value
Minimum high level input voltage	3.5 V
Maximum low level input voltage1	1.5 V
Absolute maximum input voltage	5.0 V
Absolute minimum input voltage	0.0 V
Even pins in input mode	Pulled low to 0.6 V with 17 kΩ
Odd pins in input mode	Pulled high to 4.9 V with 18 kΩ
Input time delay (typ)	137 ns

Parameter		Value
Output voltage high (typ)	Iout = -0.0 mA	5.0 V
	Iout = -10.0 mA	4.3 V
	Iout = -20.0 mA	3.6 V
	Iout = -35.0 mA	2.6 V
Output voltage low (typ)	Iout = 0.0 mA	0.0 V
	Iout = 10.0 mA	0.7 V
	Iout = 20.0 mA	1.4 V
	Iout = 35.0 mA	2.5 V

Table 5 Electrical properties of GPIO pins in differential mode

Parameter		Value
Differential input threshold voltage (typ)1		-30 ... -70 mV
Differential input threshold voltage (max)2		-200 ... + 200 mV
Maximum differential input voltage		±5 V
Absolute maximum input voltage to gnd		5.0 V
Absolute minimum input voltage to gnd		0.0 V
Common mode voltage to gnd if not limited by absolute max/min input voltage		0.0 ... 5.0 V
Differential voltage in input mode (typ) due to pull-up and pull-down resistors		4.3 V
Differential input resistance (typ)		24 kΩ
Even pins in input mode		Pulled low to 0.4 V with 18 kΩ
Odd pins in input mode		Pulled high to 4.8 V with 16 kΩ
Input time delay (typ)		149 ns
Differential output voltage high (typ)	Iout = 0.0 mA	4.1 V
	Iout = 10.0 mA	2.8 V
	Iout = 20.0 mA	2.3 V
	Iout = 35.0 mA	1.6 V

3.2.2.1 IFDR10 inputs

All IFDR10 inputs are on SMA connectors. The IF signal input is made immediately after the STALO mixing/sideband filtering step of the receiver. The required signal level for both the IF signal and burst is +11.2 dBm for the strongest expected input signal.

You can use a fixed attenuator or IF amplifier to adjust the signal level to be in this range. The maximum signal level is 16 dBm.

Table 6 IFDR10 inputs and outputs

Input	Description
IF signals	IFDR10 has 6 Rx input channels for IF signals: **Rx 0** - **Rx 5**. The user can select which channels are used for primary and secondary polarization IF signals and for wide dynamic range.
IF burst pulse sample for magnetron	Received over **ADC−E**.
Trigger input or output	2 trigger outputs on SMA connectors: **Trig 0** and **Trig 1** (50 Ohms / 4 V). 4 trigger inputs in the GPIO panel

Digitizing is performed for both the IF signal and burst channels from a user-selectable sampling frequency range of 190 ... 240 MHz at 16-bit resolution to sub-nanosecond accuracy. This provides 92 ... 107 dB of dynamic range (depending on pulse width) without using complex AGC, dual A/D ranging, or down-mixing to a lower IF frequency. Each A/D converters is time synced within 1 nanosecond to ensure sampling in multiple channels is of the nearly equivalent targets.

RVP10 provides AFC support for tuning the STALO of a magnetron system. Alternatively, the magnetron can be tuned by a motorized tuning circuit controlled by RVP10.

3.2.3 IFDR10 power, size, and mounting considerations

Table 7 IFDR installation considerations

Consideration	Description
Communication	The IFDR communicates with a host computer through 10Gb Ethernet. The Auto-MDIX feature eliminates concerns about cross-over versus straight cables. The platform provides support for TCP and UDP packets. The default IP address, shipped with each system, is 10.0.3.254. The IFDR supports jumbo packets. Vaisala recommends the UDP packet sizes be set to 8192 on the host computer. To comply with industry standards, use a shielded CAT5e cable (certified to 350 MHz), with shielded RJ45 plugs on each end. Ensure the Ethernet connectors on the host computer and IFDR make contact with the metal on the shielded cable, which provides DC return path. This design prevents ground loop currents from flowing between units, even when they are plugged into different AC/Mains.
Cooling	The unit is cooled by direct conduction of heat through the metal chassis. One side of IFDR10 serves as a heat sink. The hotter chips mounted on the printed circuit board are bonded to the heat sink. Position IFDR10 so that air can freely convect around it. A minimum of 0.6 m^3/min of air flow required. The ambient air temperature range is -40 ... +55 °C (-40 ... +131 °F).
Filters	Reserve mounting space for the external, analog, anti-alias filters. The filters can be mounted nearby in the radar cabinet, or they can be attached directly to the IFDR, on the opposite side from the power module.
Mounting	The unit is designed to be mounted on an edge. The IFDR is a compact sealed module with dimensions 246 mm × 136 mm × 51 mm (9.7 in × 5.4 in × 2.0 in). With the mounting bracket, the length of the module is 270 mm (10.6 in) and height 52.5 mm (2.1 in). See IFRD10 technical drawings (page 32).
Power	Nominal operating voltage is 24 VDC. Operating voltage range is 20 ... 30 VDC. Typical power consumption is 36 W.

3.2.4 Installing IFDR10

When installing IFDR10, note the following:

1. Mount the device so that the connectors are easy to access.
2. When connecting the cables, clean the connectors carefully with suitable tools.
3. Tighten the coaxial SMA connectors to 0.57 Nm with a torque wrench.

   It is important that the connectors are in the correct tightness.
4. When using insulated sleeves, use ferrules with 10 mm contact length.

3.3 RVP10SRV signal processing computer

The RVP10SRV signal processing computer hosts the Linux operating system and provides the computing resources for processing the I/Q values that are generated by IFDR10.

3.3.1 LAN connection for data transfer or parallel processing

For external communication, RVP10SRV supports a standard 1 Gbit Ethernet.

For communication between RVP10SRV and IFDR10, there is a 10 Gbit fiber optic cable connection.

For most applications, the IRIS Radar software is installed on the same server with RDA software. Moment results (`Z`, `T`, `V`, and `W`) are transferred internally.

The Ethernet is used to transfer moment results (`Z`, `T`, `V`, and `W`) to third-party application host computers, such as a product generator.

IFDR10 communicates over 100 Base T or 10-Gigabit Ethernet using UDP packets to send the `I` and `Q` values to RVP10SRV, and can broadcast them - allowing for archiving or parallel processing.

The digital `I` and `Q` data produced by IFDR10 is sent to the RVP10SRV server to perform the processing using pulse pairs, Fourier transforms, or random phase techniques.

3.3.2 Open hardware and software design

RVP10SRV is an open-architecture radar signal processor. The RVP10 software runs on AlmaLinux operating system.

Using public APIs, researchers and OEM manufacturers can modify or replace existing algorithms, or write their own software using the RVP10 software as a foundation.

To support software upgrades, RVP10SRV can flash IFDR10 software. The RDA version can be updated in the field with minimal risk. RVP10SRV software provides a configuration interface. For more information, see *IRIS and RDA Software Installation Guide (M212924EN)*.

3.3.3 RVP10 socket interface

RVP10SRV is configured to listen on a network port. It is ready to interface to a host computer through the network using the **DspExport** program. When the IRIS Radar software is installed on the same RVP10SRV computer, it is pre-configured to communicate with RVP10SRV processes through the native interface, bypassing the socket interface.

RVP10SRV includes built-in utilities such as **Setup**, **dspx**, and **Ascope**. See *IRIS and RDA Utilities Guide (M212925EN)*.

Because RVP10SRV can only have one program controlling it at a time, using a local program such as **dspx** blocks network access.

3.3.4 RVP10SRV socket protocol

The socket interface supports the commands in appendix *RVP10 programming interface*.

All messages going both ways consist at the lowest level of an 8-character decimal ASCII number, followed by a block of data. The decimal number indicates how many bytes follow. Generally, all data transfers are initiated by the host computer by sending a block of data, consisting of a command word followed by the | character, followed by optional data.

It responds to all commands with either an `Ack|`, indicating acknowledgment that the command was `OK`, or `Nak|`, indicating that there was an error. For `Nak|`, the reply always includes a string indicating what the error was. For Ack, there is optional data following.

On initial socket connection request **DspExport** provides a response of either `Nak|`, indicating the connection failed and why, or `Ack|`, followed by some connection information. The`Ack|` string is in the form of name/value pairs, for example:

```
Ack|CanCompress=1,Model=RVP10,Version=10.0
```

Your program can evaluate, or ignore, these keywords. `CanCompress=1` indicates that the **DspExport** computer supports compression. The host computer can then choose to use compression. When you first connect, you are in the "info only" mode. This means that the server only responds to **INFO** and **OPEN** commands.

DspExport supports the following commands:

- Read command (**READ**)
- Write command (**WRIT**)
- Read Status command (**STAT**)
- Set Information command (**INFO**)
- Read data available command (**RDAV**)
- Open the connection for I/O (**OPEN**)

Table 8 Socket protocol commands

Command	Example
Read (**READ**)	Example: `READ|100|` means: Read 100 bytes from the RVP10. Since the RVP10 interface is a 16-bit word interface, these read sizes should always be even. This command returns a `Ack|` followed by 100 bytes of binary data, or with a `Nak|`, meaning there can be no partial reads.
Write (**WRIT**)	Example: `WRIT|<data>`, where `<data>` is some binary data. This data is written to RVP10. The data size should be even.
Read Status (**STAT**)	Example: `STAT|` reads the status bits back from the RVP10. This is a 1-bit value, set to **1** if RVP10 has data available in its output buffer. The command returns `Ack|0`, `Ack|1`, or `Nak`. This is equivalent to the `dspr_status()` call in the `dsp` library.
Set Information (**INFO**)	Example: `INFO|ByteOrder=LittleEndian,WillCompress=1,Version=10.0`. This command can be used to inform RVP10SRV `DspExport` about the host computer. Available options are: • `ByteOrder`—Informs `DspExport` of the byte order of the host computer. This is needed because all the data read or written to/from the RVP10 is in 16-bit words. If the host computer has a different byte order from the RVP10, DspExport byte swaps the data. • `WillCompress`—Informs `DspExport` to use compression or not. Compression is only used if both sides agree to use it. The host computer should only set this to 1 if it received a `CanCompress` of 1 on initial connection. The data from normal **READ** commands is compressed. If the data is compressed, it replies with the acknowledge compressed string of `AkC`. The compression program is the `zlib` compress and uncompress. The uncompress function requires that the caller know the expected uncompressed size. This is true for RVP10 reads, because the reader always specifies the read size. • `Version`—Sends the IRIS version.
Read Data Available (**RDAV**)	Example: `RDAV|100|2|` means read up to 100 bytes of data from the RVP10SRV in individual DMA transfers of 2 bytes each. Before each read, the status is checked to see if there is more data available. If not, the read stops, and the number of bytes read is returned. This is merely a performance enhancing command, since the same feature is available by using the **READ**and **STAT** commands.

Command	Example
Open the Connection for I and O (**OPEN**)	Example: **OPEN** means: Switch from "open to info only" mode to open for I/O. If the signal processor is in use by another device, this command returns an error. Multiple clients are allowed to connect for info only, but only one can do I/O. If you run `DspExport` with the `-803` command line option, you get the legacy behavior, which means that every connection automatically sends the **OPEN** command. There is no reverse command to switch back to open for info only. There is also no such library call in the driver.
Read **Zcal** Information (**RCAL**)	Example: `ZCAL` means: Read the `dsp_refl_cal` structure from RVP10 and send it back in an ASCII name=value pair format. This is the structure configured by **Zauto** and **Zcal**. The configuration is served to all clients using RVP10.
Reset Kernel FIFOs (**RKFF**)	Example: `RKFF|2|` means: Reset the kernel FIFOs on the RVP10. The argument specifies which direction FIFOs to reset.
Read **Setup** Information (**SETU**)	Example: `SETU` means: Read the `dsp_manual_setup` structure from RVP10 and send it back in an ASCII `name=value` pair format. This is the structure configured in the RVP section of the **Setup** utility. The configuration is served to all clients using RVP10.
Write **Zcal** Information (**WCAL**)	Example: `WCAL|...` writes the `dsp_refl_cal` structure to RVP10 for saving.

3.3.5 Public API

To support writing your own signal processing algorithms for RVP10, the RVP10 software architecture enables you to statically link plug-in modules to the running code. The following table shows how the API supports adding software extensions to the RVP10 framework to modify some signal processing stages.

Table 9 API support for modifying signal processing

Processing stage	API support
Tx/Rx waveform synthesis and matched filter generation	Define transmit waveforms from pulse-to-pulse, along with the corresponding FIR coefficients that extract (`I`,`Q`) from the Tx waveform. Allows users to experiment with arbitrary waveforms for pulse compression and frequency agility.
Time series and spectra processing from (`I`,`Q`)	Modify default time series and spectra data, for example, to perform averaging or windowing in a different way.

Processing stage	API support
Parameter generation from (`I`,`Q`)	• Redefine how standard parameters (`dBZ`, `Velocity`, `Width`, `PHIDP`, and so on) are computed from the incoming (`I`,`Q`) time series. • Create new parameter types.

The standard scientific algorithms are not public. Many RVP10 library routines are also documented and can be called by user code, but the source to these routines is not generally released. Development tools must be purchased separately.

3.3.6 Installing the RVP10SRV server computer

WARNING! The RVP10SRV server computer has two power supplies. Disconnect power from both power supplies when powering down or servicing the unit.

1. Mount the RVP10SRV server chassis in an equipment rack on rack slides.
2. Use the fiber optic cable to connect IFDR10 to the RVP10SRV server chassis.

   Clean the connectors carefully with appropriate tools. If the connectors are not properly cleaned, the data quality may suffer.
3. Connect the power cables.

   The device includes dual-redundant power supplies, with two line cords.

3.3.6.1 Powering up RVP10SRV

1. Power-up and boot IFDR10.

   If IFDR10 is not powered-up and booted, the `rvp10` process cannot start on RVP10SRV.
2. Start or reset RVP10SRV.

   The host Linux PC goes through an automated boot process that ultimately starts the RVP10 application.
3. While RVP10SRV runs extensive internal diagnostics, if no display is connected yet, you can connect a display to view any error messages or monitor the startup log in */var/log/irisrda/rvp10.log*.

3.4 Configuring network interface from RVP10SRV to IFDR10

This chapter describes how to configure the network interface from RVP10SRV server to IFDR10.

Configure the following parameters in the *profile.conf* file, located in */etc/vaisala/irisrda/profile.conf*.

```
IP Adress of networked RVP10/IFD IQ stream
```

The parameter **IP Adress of networked RVP10/IFD IQ stream** defines the Ethernet address of the source IFDR10's IQ data stream. For the best results, attach the IFDR to a dedicated Ethernet port of the host computer with no routers, switches, or hubs in between.

```
Port of networked RVP10/IFD IQ stream
```

The parameter **Port of networked RVP10/IFD IQ stream** sets the port, or unique identification of the RDA application running on the IFDR10 IP address location.

```
IP address of networked RVP10/IFD gRCP
```

The question **IP address of networked RVP10/IFD gRPC** defines the Ethernet address where the RVP10 server finds the IFDR10's gRPC control interface.

```
Port of networked RVP10/IFD gRCP
```

The parameter **Port of networked RVP10/IFD gRPC** provides the RVP10 server the unique port identification of the IFDR10's controlling application.

Example of *profile.conf*:

```
install_usr_root=/usr
install_etc_root=/etc
data_root=/srv/iris_data
log_root=/var/log
network_port="TCP 30725"
operator=operator
operators="radarop operator sipan admin root"
observers="observer"
tsexport_port=30780
tsimport_port=30781
tsexport_ip=192.168.76.36
ifdr10_iq_stream_ip_addr=10.0.3.254
ifdr10_iq_stream_port=1001
ifdr10_grpc_ip_addr=10.0.2.254
ifdr10_grpc_port=5000
```

3.5 STALO control

The earlier generations of Vaisala RVPs used a legacy Sigmet digital automatic frequency control (DAFC) device for STALO control. RVP10 is using a new approach with off-the-shelf industrial automation products for STALO control. For controlling STALOs having RS-422 serial data interfaces, the Moxa NPort IA5150AI-T device is used. It receives control commands over the internal radar network from the RVP10 server, and converts them to RS-422 serial output. Currently, this is the only method provided for controlling STALOs, but other methods can be implemented on request.

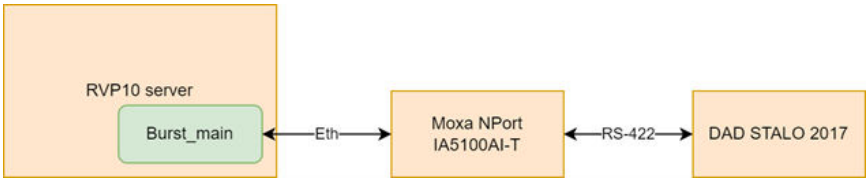

Figure 5 STALO control

4. Technical specifications

4.1 Signal processing

Table 10 Signal processing

Feature	Description
Signal processor	Vaisala RVP10
Azimuth averaging	2–1024 pulses
IF digitizing	16 bits
Clutter filters	Fixed/Adaptive GMAP in frequency domain, or IIR time domain
Data outputs (8 and 16 bit)	`Ah/v`, `Azdr`, `CCOR`, `CSP`, `CSR`, `dBT`, `dBZ`, `dBZt`, `KDP`, `LDR`, `LOG`, `PHIH/V`, `PHIDP`, `PMI`, `R`, `RHOHV`, `SNR`, `SQI`, `T`, `V`, `VC`, `W`, `Z`, `ZC`, `ZDR`, `ZDRC`, `Zh`, `Zv`, `Zhv`
Optional data outputs	`HCLASS`, `I/Q`
Dual-polarization	Simultaneous, H only, V only
Dual PRF velocity de-aliasing	2:3, 3:4, or 4:5 for 2X, 3X, or 4X velocity unfolding
Enhanced reflectivity processing (Zhv)	> 3 dB improvement detection gain
Processing modes	PPP, FFT/DFT, Random phase coding / SZ 8/64 phase coding for 2nd trip filtering and recovery
Maximum number of range bins	Full unambiguous range at minimum resolution, or more than 8192 range bins per channel (whichever is less)
Minimum range resolution	Down to 15 m (accuracy of ±1.0 m).
Maximum range	Up to 1024 km

4.1.1 Processing algorithms

Table 11 Processing algorithms

Algorithm	Description
`I/Q` signal correction options	• Amplitude jitter correction based on running average of transmit power from burst pulse • Interference correction for single pulse interference • Saturation correction (3 ... 5 dB)

Algorithm	Description
Primary processing modes	• Poly-Pulse Pair (PPP) • DFT • Random or phase coded second trip echo filtering/recovery • Optional polarization with full co-variance matrix (**Zdr**, **PHIDP**, **LDR**, **RHOHV**, and so on) • Optional pulse compression
Processing options	• Azimuth averaging: 2 ... 1024 pulses • Corrections for gaseous attenuation and1/R2 • Dual-polarization: Alternating, Simultaneous, H-only, V-only • Clutter filters: Fixed/Adaptive GMAP in frequency domain, or IIR time domain • High sensitivity Rhv STAR mode processing: >3dB improvement in detectability • Pulse integration up to1024 • Range de-aliasing: random phase • Scan angle synchronization for data acquisition • Up to 4 pulse widths • Velocity de-aliasing: dual PRF velocity unfolding at 2:3, 3:4, and 4:5 for 2X, 3X, or 4X velocity unfoldings
Data outputs (8 and 16 bit)	**Zh**, **Zv**, **Zhv**, **V**, **W**, **SQI**, **ZDR**, **LDR**, **RHOHV**, **PHIDP**, and **KDP**
Optional data outputs	**HCLASS**, **I/Q**
Data quality thresholds	• Signal-to-noise ratio (SNR)—Used to reject bins having weak signals; typically applied to dBZ • Signal quality index (SQI)—Used to reject bins having incoherent signals; typically applied to mean velocity and width • Clutter-to-signal ratio (CSR)—Used to reject range bins having very strong clutter; typically applied to mean velocity, width, and dBZ • Speckle Filter—Removes single-bin targets such as aircraft or noise and fills isolated missing pixels

4.2 RVP10 Input and output summary

Table 12 I/O summary

Function	Description
AZ/EL angle input options	• Serial **AZ/EL** angle tag input using standard Vaisala RCP format • 16-bit each parallel TTL binary angles through the I/O-62 card • Synchro angle inputs through the I/O-62 card • RCP network antenna packet protocol

Function	Description
Ethernet I/O from host computer	Data output of calibrated **dBZ**, **V**, and **W** during normal operation. Full **I/Q** time series recording with a separate tsarchive utility, or through a custom application using a public API. Signal processor configuration and verification read-back is performed through the Ethernet interface.
Input from IFDR	• 32-bit floating point **I/Q** values • Optional dual-channel **I/Q** samples (for example, for polarization systems or dual-frequency systems)
Optional polarization control	RS-422 differential control for polarization switch
Trigger output	Up to 12 total triggers available on various connector pins. Triggers are programmable with respect to trigger start, trigger width, and sense (normal or inverted).

4.3 IFDR10 specifications

Table 13 IF bandpass filter

Function	Description
IF bandpass filter	Programmable digital FIR with software-selectable bandwidth, including pulse compression. Built-in filter design software with user interface.

Table 14 IF inputs

Characteristic	Description
A/D and D/A conversion	Resolution: 16 bit Sampling rate: 190 ... 240 MHz (software-selectable)
Dynamic range (dependent on matched filter)	104 dB without compression (1 µs pulse) 107 dB without compression (2 µs pulse)
IF range	10 ... 120 MHz
Input signals	• IF received signal: 50 Ω, +12.0 dBm full-scale, absolute max +20 dBm • IF burst or STALO: 50 Ω, +12.0 dBm full-scale, absolute max +20 dBm • Optional reference clock: 9 – 700 MHz with 0.5 MHz, 9.0 dBm ... +19.0 dBm

Characteristic	Description
Master clock jitter	< 0.5 picosec, integrated over 200 Hz ... 2 MHz offset
Multiply/accumulate cycles per second	448 billion
Pulse repetition frequency (PRF)	50 Hz ... 20 kHz, +0.1 %, continuously selectable
Saturation level (1 dB compression)	+13.3 dBm at 50 Ω

Table 15 Digital waveform synthesis

Characteristic	Description
Analog waveform applications	• Digitally synthesized IF transmit waveform for pulse compression, frequency agility, and phase modulation applications. • Master clock or STALO signal to the radar, either phase-locked or free-running frequency.
TxDAC analog output waveform characteristics	Two independent, digitally synthesized, analog output waveforms (SMA) Max output power +10 dBm Frequency range 10 MHz ... 120 MHz

Table 16 RVP10 I/O

Characteristic	Description
Inputs (IFDR10)	Only digital inputs
Data output through Ethernet (IFDR10)	32-bit floating point I and Q values
I/O interface (IFDR10)	8 independent GPIO pairs Each pair can be configured as one differential input/output, or as two single-ended inputs/outputs (max 16 single-ended lines)
AFC output (RVP10SRV)	Serial control output Automatic 2D (time/frequency) burst pulse search and fine-tracking algorithms
IFDR10 to RVP10SRV link	Optical link (10 Gbit)

Table 17 Electrical properties of GPIO pins in single-ended input mode

Charasteristic	Description
Minimum high level input voltage	3.5 V
Maximum low level input voltage	1.5 V
Absolute maximum input voltage	5.0 V
Absolute minimum input voltage	0.0 V

Table 18 Electrical properties of GPIO pins in single-ended output mode

Charasteristic	Description
Output voltage high	5.0 V (I out = 0 mA)
	4.3 V (I out = -10 mA)
	3.6 V (I out = -20 mA)
Output voltage low	0.0 V (I out = 0 mA)
	0.7 V (I out = 10 mA)
	1.4 V (I out = 20 mA)

Table 19 Electrical properties of GPIO pins in differential mode

Characteristic	Decription
Differential input threshold voltage	-200 ... +200 mV
Absolute maximum and minimum differential input voltage	±5 V
Absolute maximum input voltage to gnd	5.0 V
Absolute minimum input voltage to gnd	0.0 V
Common mode voltage to gnd if not limited by absolute max/min input voltage	0.0 ... 5.0 V
Typical differential output voltage high	4.1 V (I out = 0 mA)
	2.8 V (I out = 10 mA)
	2.3 V (I out = 20 mA)
Typical differential output voltage low	-4.1 V (I out = 0 mA)
	-2.8 V (I out = 10 mA)
	-2.3 V (I out = 20 mA)

The differential GPIO voltage of a pin pair is defined as *the Odd pin voltage minus the Even pin voltage*. For example, if **`GPIO1 = 2 V`** and **`GPIO0 = 0.3 V`**, the differential GPIO voltage is **`2 V – 0.3 V = 1.7 V`**, and the differential pin state is true.

4.4 IFDR10 physical and environmental characteristics

Table 20 Physical and environmental characteristics

Characteristic	Description
Dimensions (w × l × h)	246 mm × 136 mm × 51 mm (9.7 in × 5.4 in × 2.0 in) With mounting brackets: 270 mm × 136 mm × 52.5 mm(10.6 in × 5.4 in × 2.1 in)
Input power	20 ... 30 VDC
Power consumption	Typical: 36 W ± 10 %
Environment	-40 °C ... +55 °C (-40 °F ... +131°F) 0 %RH ... 95 %RH (non-condensing) with a minimum airflow of 0.6 m^3/min
Reliability (IFDR10)	MTBF > 50,000 hours (at 25 °C) < 1 hour MTTR

4.5 RVP10SRV signal processing computer specifications

Table 21 Physical and environmental characteristics

Characteristic	Description
Chassis	• 3U Short-depth rackmount chassis (depth 18.9"), Advantech HPC-7320 Chassis • Rack rail kit to accommodate 19" racks of depths 18" ... 36"
Cooling	• Fan: 2 (8 cm/57CFM) + 1 (6 cm/27.72CFM) • Air filter

Characteristic	Description

I/O	• PCI slot to allow for IO-62 card installation
	• DVD +/-RW drive
	• 2 Serial ports accessed from the back
	• 10 Gb Ethernet port accessed from the back
	• 3.0 USB ports
	  • 4 ports accessed from the back
	  • 2 ports accessed in the front
	• 2.0 USB ports, accessed from the back
	• PS/2 Single Connector with brake out cable for monitor and keyboard

Memory and processing	• 512 GB Solid State Drive configured with RAID 1 (mirrored) • 16 G of DDR4 Memory • 2 XEON E5-2609 v3 Processors with 6 Cores, 1.9G Hz clock speed, 6.4GT/s QPI Speed, 15M of Cache
Non-operating environment	Temperature: -40 ... +70° C (-40 ... +156° F) Humidity: 10 ... 95% at 60° C, non-condensing Vibration (5 ... 500Hz): 2 G
Operating environment	Temperature: 0 ... +40° C (32 ... +122° F) Humidity: 10 ... 95% at 40° C, non-condensing Vibration (5 ... 500Hz): 1 Grms Shock: 10 G (with 11 ms duration, half sine wave)
Physical characteristics	Dimensions (W * H * D): 426.4 * 132.2 * 480 mm (16.79″ * 5.2″ * 18.9″) Weight: 13.7 kg (30.1 lbs)
Power	Dual redundant power supplies auto-ranging 100 ... 240 V AC

4.6 Regulatory statements

Table 22 Regulatory statements for IFDR10

EU Directive	Standard
EMC Directive (2014/30/EU)	EN 61326-1:2013, Electrical equipment for measurement, control and laboratory use - EMC requirements - Part 1: General requirements. IFDR10 fulfills the requirements for Class B equipment.
Eye safety	Class 1 laser product, IEC/EN 60825-1:2014
Compliance marks	CE, UKCA

The following list of standards applies to the Advantech HPC-7320 server computer as manufactured. If any configurations are done to the server after manufacturing, the list may no apply.

Table 23 Regulatory statements for RVP10SRV

Item	Standard
EMC Directive (2014/30/EU)	
	IEC/EN 61000-6-4, Generic standards
	EN55011, Class A, Group 1 CISPR 32 / EN 55032, Class A
	EN 55024:2010+A1:2015 EN 55035:2017+A11:2020
	EN61000-3-2 / EN61000-3-3, harmonics and flicker
	EN61000-6-2, electromagnetic compatibility
	IEC/EN 61000-4-2, electrostatic discharge immunity
	IEC/EN 61000-4-3, radiated RF-field immunity
	IEC/EN 61000-4-4, electrical fast transient immunity
	IEC/EN 61000-4-5, surge immunity
	IEC 61000-4-6, conducted RF-field immunity
	EN 61000-4-8, testing and measurement techniques
	IEC 61000-4-11, voltage dips and short interruptions immunity
Compliance marks	CE

4.7 RVP10 spare parts

Table 24 IFDR10 spare parts

Part number	Description
IFDR10SP	Intermediate Frequency Digital Receiver without software
270934SP	SFP+ fiber optic module TX1271 for IFDR10
223150SP	Bandpass filter 30 MHz with coaxial cable
223151SP	Bandpass filter 60 MHz with coaxial cable
223152SP	Bandpass filter 57.5 MHz with coaxial cable
271595SP	Fiber optic cable, simplex SM, LC to LC, 5m

Part number	Description
260799SP	Power suppy AC/DC 24VDC for IFDR10

Table 25 RVP10SRV computer spare parts

Part number	Description
RVP10SRVSP	Signal prosessing computer
270935SP	10G optical Ethernet SFP+ module
RCP8-CPSP	IO62 panel RCP8
RVP8-IOSP	IO62 card
248382SP	Power supply for RVP10SRV

Appendix A. IFRD10 technical drawings

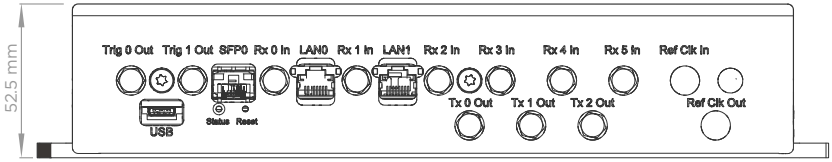

Figure 6 IFDR10 front view

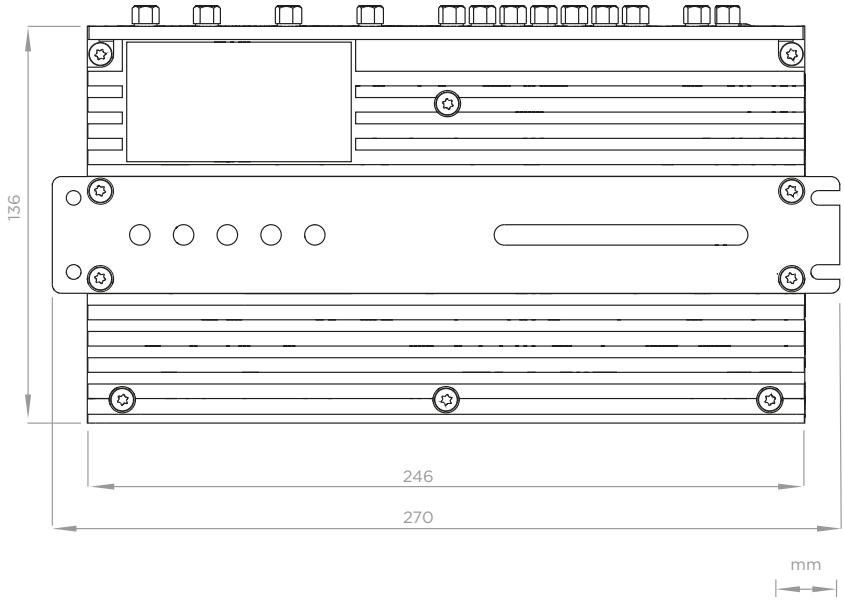

Figure 7 IFDR10 bottom view

Appendix B. Recycling instruction

These recycling instructions guide you on the end-of-life treatment of this Vaisala product. As waste regulations and infrastructure vary in each country, these instructions only indicate the different components to be separated and common ways to handle them. Always follow local requirements when disposing of the product. Vaisala encourages to use the best available recycling practices to minimize related environmental impacts.

Vaisala is committed to meeting the requirements of the EU Waste Electrical and Electronic Equipment (WEEE) Directive. This directive aims to minimize the impact of electrical and electronic goods on the environment, by increasing reuse and recycling, and reducing the amount of WEEE going to landfill. This symbol indicates that the product should be collected separately from other waste streams and treated appropriately.

For recycling the RVP10SRV server, see manufacturer's documentation.

IFDR10 includes an aluminium chassis, which must be disposed of as metal waste, and a circuit board that must be disposed of as electrical/electronic waste.

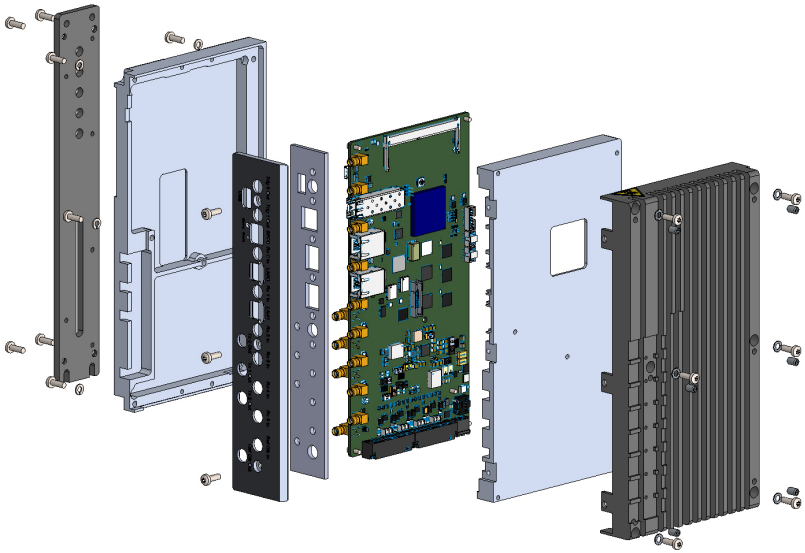

Figure 8 IFDR10 exploded view

Warranty

For standard warranty terms and conditions, see vaisala.com/warranty.
Please observe that any such warranty may not be valid in case of damage due to normal wear and tear, exceptional operating conditions, negligent handling or installation, or unauthorized modifications. Please see the applicable supply contract or Conditions of Sale for details of the warranty for each product.

Technical support

Contact Vaisala technical support at helpdesk@vaisala.com. Provide at least the following supporting information as applicable:

- Product name, model, and serial number
- Software/Firmware version
- Name and location of the installation site
- Name and contact information of a technical person who can provide further information on the problem

For more information, see vaisala.com/support.

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