

# Table of Contents

<b>Hardware Limited Warranty .....</b>	<b>ix</b>
<b>Preface .....</b>	<b>x</b>
<b>1. Introduction and Specifications .....</b>	<b>1-1</b>
1.1 System Design Concept .....	1-2
1.2 RVP7 Digital Receiver Processing Advantages .....	1-4
1.2.1 What is a Digital IF Receiver? .....	1-4
1.2.2 Reduced Initial Cost .....	1-4
1.2.3 Reduced Life Cycle Cost .....	1-4
1.2.4 Performance and Flexibility Examples .....	1-5
1.3 Comparison of Analog vs Digital Radar Receivers .....	1-7
1.3.1 Magnetron Receiver Example .....	1-7
1.3.2 Klystron Receiver Example .....	1-9
1.4 Digital IF Front End Processing .....	1-10
1.4.1 Burst Pulse Analysis for Amplitude/Frequency/Phase .....	1-10
1.4.2 Main Board IF Signal Processing .....	1-10
1.5 RVP7 Weather Signal Processing .....	1-12
1.5.1 General Processing features .....	1-12
1.5.2 RVP7 Pulse Pair Processing .....	1-15
1.5.3 RVP7 FFT Processing .....	1-16
1.5.4 Doppler Doubler – Random Phase Processing .....	1-16
1.5.5 Output Data .....	1-17
1.6 RVP7 Control and Maintenance Features .....	1-18
1.6.1 Radar Control Options .....	1-18
1.6.2 Local TTY and Scope Setups .....	1-18
1.6.3 Built-In Diagnostics .....	1-19
1.7 Support Software .....	1-20
1.8 RVP7 Technical Specifications .....	1-21
1.8.1 IFD Digitizer Module .....	1-21
1.8.2 Digital “I” and “Q” Synthesis .....	1-21
1.8.3 Computed Weather Parameters .....	1-22
1.8.4 Processing Speed and RVP7/AUX Option .....	1-22
1.8.5 Clutter Filters .....	1-23
1.8.6 Data Thresholds .....	1-23
1.8.7 Other Data Outputs and Features .....	1-23
1.8.8 Real Time Display Serial Stream .....	1-24
1.8.9 External Trigger Input .....	1-24
1.8.10 Internal Trigger Generator .....	1-24

1.8.11 Host Computer Interface .....	1-25
1.8.12 Radar Control Signals .....	1-25
1.8.13 Physical and Environmental .....	1-25
<b>2. Hardware Installation .....</b>	<b>2-1</b>
2.1 IFD IF Digitizer Module .....	2-1
2.1.1 Input A/D Saturation Levels .....	2-2
2.1.2 IF Bandwidth and Dynamic Range .....	2-2
2.1.3 IF Gain and System Performance .....	2-4
2.1.4 Choice of Intermediate Frequency .....	2-7
2.1.5 AFC Output Voltage (Optional) .....	2-7
2.1.6 Reference Clock Input (Optional) .....	2-8
2.1.7 Coax Uplink and Fiber Downlink .....	2-9
2.1.8 Adjustments and Indicators .....	2-10
2.1.9 Size and Mounting Considerations .....	2-11
2.2 RVP7/Main Board and Chassis .....	2-13
2.2.1 Power-Up Details .....	2-13
2.2.2 Booting Code Upgrades From IRIS .....	2-14
2.2.3 Radar Digital Signals .....	2-15
2.2.4 Backpanel Digital AFC Outputs .....	2-18
2.2.5 SCSI Interface Signals .....	2-18
2.2.6 Parallel Interface Signals .....	2-20
2.2.7 Jumper Settings .....	2-20
2.2.8 RVP7/Main Board Pin Assignments .....	2-22
2.3 RVP7 Auxiliary Processing Board (RVP7/AUX) .....	2-25
2.4 Digital AFC Module (DAFC) .....	2-26
2.4.1 Example Hookup to a CTI "MVSR-xxx" STALO .....	2-28
2.4.2 Example Hookup to a MITEQ "MFS-xxx" STALO .....	2-30
2.5 RVP7 Custom Interfaces .....	2-31
2.5.1 Using the IFD Coax Uplink .....	2-31
2.5.2 Using the (I,Q) Digital Data Stream .....	2-34
<b>3. TTY Nonvolatile Setups .....</b>	<b>3-1</b>
3.1 Overview of Setup Procedures .....	3-1
3.1.1 Initial Entry and Help List .....	3-1
3.1.2 Factory, Saved, and Current Settings .....	3-2
3.1.3 Processor Reset Command .....	3-3
3.1.4 V — View Internal Status .....	3-4
3.1.5 Burst-In / IF-In Swap Command .....	3-7
3.2 Host Computer I/O Debugging .....	3-8
3.2.1 Physical-Level I/O Examiner .....	3-8
3.2.2 Application-Level I/O Examiner .....	3-8
3.3 View/Modify Dialogs .....	3-11

3.3.1	Mc — Board Configuration .....	3-11
3.3.2	Mp — Processing Options .....	3-16
3.3.3	Mf — Clutter Filters .....	3-20
3.3.4	Mt — General Trigger Setups .....	3-22
3.3.5	Mt<n> — Triggers for Pulsewidth #n .....	3-24
3.3.6	Mb — Burst Pulse and AFC .....	3-29
3.3.6.1	AFC Motor/Integrator Option .....	3-36
3.3.7	M* — Standalone Settings .....	3-37
3.3.8	M+ — Debug Options .....	3-39
3.3.9	Mz — Transmitter Phase Control .....	3-41
<b>4.</b>	<b>Plot-Assisted Setups .....</b>	<b>4-1</b>
4.1	Oscilloscope Connections .....	4-2
4.2	P+ — Plot Test Pattern .....	4-3
4.3	General Conventions Within the Plot Commands .....	4-4
4.4	Pb — Plot Burst Pulse Timing .....	4-6
4.4.1	Interpreting the Burst Timing Plot .....	4-6
4.4.2	Available Subcommands Within “Pb” .....	4-7
4.4.3	TTY Information Lines Within “Pb” .....	4-8
4.4.4	Recommended Adjustment Procedures .....	4-9
4.5	Ps — Plot Burst Spectra and AFC .....	4-11
4.5.1	Interpreting the Burst Spectra Plots .....	4-11
4.5.2	Available Subcommands Within “Ps” .....	4-13
4.5.3	TTY Information Lines Within “Ps” .....	4-15
4.5.4	Computation of Filter Loss .....	4-17
4.5.5	Recommended Adjustment Procedures .....	4-20
4.6	Pr — Plot Receiver Waveforms .....	4-23
4.6.1	Interpreting the Receiver Waveform Plots .....	4-23
4.6.2	Available Subcommands Within “Pr” .....	4-25
4.6.3	TTY Information Lines Within “Pr” .....	4-26
<b>5.</b>	<b>RVP7 Processing Algorithms .....</b>	<b>5-1</b>
5.1	IF Signal Processing .....	5-4
5.1.1	FIR (Matched) Filter .....	5-4
5.1.2	Automatic Frequency Control (AFC) .....	5-5
5.1.3	Burst Pulse Tracking .....	5-6
5.1.4	Interference Filter .....	5-7
5.1.5	Large-Signal Linearization .....	5-9
5.1.6	Correction for Tx Power Fluctuations .....	5-9
5.2	Video (“I” and “Q”) Signal Processing .....	5-11
5.2.1	Time Series .....	5-11
5.2.2	IIR Clutter Filter for PPP-Mode .....	5-11
5.2.3	Autocorrelations for PPP-Mode .....	5-12

5.2.4	Range averaging and Clutter Microsuppression	5-13
5.2.5	Reflectivity	5-13
5.2.6	Velocity	5-15
5.2.7	Spectrum Width Algorithms	5-15
5.2.8	Signal Quality Index (SQI threshold)	5-16
5.2.9	Clutter Correction (CCOR threshold)	5-17
5.2.10	Weather Signal Power (SIG threshold)	5-18
5.2.11	Signal to Noise Ratio (LOG threshold)	5-18
5.3	Thresholding	5-19
5.3.1	Threshold Qualifiers	5-19
5.3.2	Adjusting Threshold Qualifiers	5-20
5.3.3	Speckle Filters	5-21
5.4	Reflectivity Calibration	5-25
5.5	Dual PRT Processing Mode	5-30
5.5.1	DPRT-1 Mode	5-30
5.5.2	DPRT-2 Mode	5-31
5.6	Dual PRF Velocity Unfolding	5-32
5.7	Optional Dual Polarization- ZDR, PHIDP, KDP, LDR, ...	5-36
5.7.1	Overview of Dual Polarization	5-36
5.7.2	Radar System Considerations	5-38
5.7.3	RVP7 Dual-Channel Receiver Approach	5-40
5.7.4	Overview of Processing Algorithms	5-42
5.7.5	Case 1: Fixed Transmit: Dual-Channel Receiver	5-45
5.7.6	Case 2: Simultaneous Dual Transmit and Receive (STAR mode)	5-46
5.7.7	Case 3: Alternating H/V Transmit: Single-Channel Receiver	5-47
5.7.8	Case 4: Alternating H/V Transmit: Dual-Channel Receiver	5-48
5.7.10	KDP Calculation	5-49
5.7.11	Standard Moment Calculations (T, Z, V, W)	5-50
5.7.12	Thresholding of Polarization Parameters	5-60
5.7.13	Calibration Considerations	5-61
5.8	FFT Mode	5-64
5.8.1	Overview	5-64
5.8.2	FFT Implementation	5-65
5.9	Random Phase 2nd Trip Processing	5-72
5.9.1	Overview	5-72
5.9.2	Algorithm	5-72
5.9.3	Tuning for Optimal Performance	5-73
5.10	Signal Generator Testing of the Algorithms	5-77
5.10.1	Linear Ramp of Velocity with Range	5-77
5.10.2	Verifying PHIDP and KDP	5-78
5.10.3	Verifying RHOH, RHOV, and RHOHV	5-78

<b>6. Host Computer Commands</b>	<b>6-1</b>
6.1 No-Operation (NOP)	6-2
6.2 Load Range Mask (LRMSK)	6-2
6.3 Setup Operating Parameters (SOPRM)	6-4
6.4 Interface Input/Output Test (IOTEST)	6-10
6.5 Interface Output Test (OTEST)	6-11
6.6 Sample Noise Level (SNOISE)	6-11
6.7 Initiate Processing (PROC)	6-13
6.8 Load Clutter Filter Flags (LFILT)	6-21
6.9 Get Processor Parameters (GPARM)	6-22
6.10 Load Simulated Time Series Data (LSIMUL)	6-31
6.11 Reset (RESET)	6-33
6.12 Define Trigger Generator Output Waveforms (TRIGWF)	6-33
6.13 Define Pulse Width Control Bits and PRT Limits (PWINFO)	6-35
6.14 Set Pulse Width and PRF (SETPWF)	6-36
6.15 Load Antenna Synchronization Table (LSYNC)	6-37
6.16 Set/Clear User LED (SLED)	6-39
6.17 TTY Operation (TTYOP)	6-39
6.18 Load Custom Range Normalization (LDRNV)	6-40
6.19 Read Back Internal Tables and Parameters (RBACK)	6-41
6.20 Pass Auxiliary Arguments to Opcodes (XARGS)	6-42
6.21 Load IIR Clutter Filter Coefficients (LFCOEFS)	6-43
6.22 Configure Ray Header Words (CFGHDR)	6-43
6.23 Configure Interference Filter (CFGINTF)	6-44
6.24 Load ROM Image and Reboot (BOOT)	6-45
6.25 Set AFC level (SETAFC)	6-47
6.26 Set Trigger Timing Slew (SETSLEW)	6-47
6.27 Hunt for Burst Pulse (BPHUNT)	6-47
6.28 Configure Phase Modulation (CFGPHZ)	6-48
<b>A. Clutter Filter Characteristics</b>	<b>A-1</b>
<b>B. Real Time Display Serial Stream</b>	<b>B-1</b>
B.1 Serial Commands Received by the RVP7	B-2
B.1.1 Select Output Parameters Command (SOUTP)	B-2
B.1.2 Load Levelization Info Command (LDLEV)	B-4
B.1.3 GPARM Request (RQGPRM)	B-5
B.1.4 Sample Noise Levels (RTNOISE)	B-5
B.2 Serial Data Output by the RVP7	B-6
B.2.1 Parameter Description Packet	B-6
B.2.2 GPARM Information Packet	B-7
B.2.3 Parameter Data Packet	B-7

<b>C. Packaging</b>	<b>C-1</b>
C.1 Main Chassis General Description	C-1
C.2 Main Chassis Front Panel	C-2
C.3 Main Chassis Back Panel	C-2
C.4 RVP7/IFD Module General Description	C-3
<b>D. References and Credits</b>	<b>D-1</b>
<b>E. Installation and Test Procedure</b>	<b>E-1</b>
E.1 Installation Check	E-3
E.2 Jumper Settings	E-4
E.3 Power-Up Check	E-5
E.4 Setup Terminal	E-6
E.5 Setup "V" Command (Internal Status)	E-7
E.6 Setup "Mc" Command (Board Configuration)	E-8
E.7 Setup "Mp" Command (Processing Options)	E-9
E.8 Setup "Mf" Command (Clutter Filters)	E-10
E.9 Setup "Mt" Command (General Trigger Setup)	E-11
E.10 Initial Setup of Information for Each Pulse Width	E-12
E.11 Setup "Mb" Command (Burst Pulse and AFC)	E-13
E.12 Setup "M*" Command (Stand-alone Settings)	E-14
E.13 Setup "M+" Command (Debug Options)	E-15
E.14 Setup "Mz" Command (Transmitter Phase Control)	E-16
E.15 Display Scope Test	E-17
E.16 Burst Pulse Alignment	E-18
E.17 Bandwidth Filter Adjustment	E-19
E.18 Digital AFC Voltage Alignment (Optional)	E-20
E.19 Analog AFC Voltage Alignment (Optional)	E-21
E.20 MFC Functional Test and Tuning (Optional)	E-23
E.21 AFC Functional Test (Optional)	E-24
E.22 Input IF Signal Level Check	E-25
E.23 Dynamic Range Check	E-26
E.24 Receiver Bandwidth Check	E-28
E.25 Receiver Phase Noise Check	E-30
E.26 Hardcopy of Final Setups	E-31
<b>Index</b>	<b>Index-1</b>

## Figures

Figure 1-1: Overall Block Diagram of the RVP7 .....	1-3
Figure 1-2: Analog vs Digital Receiver for Magnetron Systems .....	1-8
Figure 1-3: Analog vs Digital Receiver for Klystron Systems .....	1-9
Figure 1-4: RVP7 Weather Processing Steps .....	1-13
Figure 2-1: Calibration Plot for a Stand-alone 14-Bit IFD .....	2-4
Figure 2-2: Tradeoff Between Dynamic Range and Sensitivity .....	2-5
Figure 2-3: Timing of pulses that contribute to each ray, relative to ENDRAY_ ..	2-17
Figure 2-4: Assembly Diagram of the DAFC .....	2-26
Figure 2-5: Recommended Receiving Circuit for the Coax Uplink .....	2-31
Figure 2-6: Timing Diagram of the IFD Coax Uplink .....	2-32
Figure 2-7: Timing diagram of the (I,Q) Data Stream .....	2-35
Figure 4-1: Oscilloscope Display of Test Pattern .....	4-3
Figure 4-2: Successful Capture of the Transmit Burst .....	4-6
Figure 4-3: Example of a Filter With Excellent DC Rejection .....	4-11
Figure 4-4: Example of a Poorly Matched Filter .....	4-20
Figure 4-5: Example of a Filter With Poor DC Rejection .....	4-22
Figure 4-6: Example of Combined IF Sample and LOG Plot .....	4-23
Figure 4-7: Example of a Noisy High Resolution "Pr" Spectrum .....	4-25
Figure 5-1: Flow Diagram of RVP7 Processing .....	5-3
Figure 5-2: Linearization of Saturated Signals Above +4dBm .....	5-10
Figure 5-3: Model Intensity Curve .....	5-25
Figure 5-4: Illustration of Losses that Affect LOG Calibration .....	5-28
Figure 5-5: Dual PRF Concepts .....	5-33
Figure 5-6: Example of Dual PRF Trigger Waveforms .....	5-35
Figure 5-7: Dual Receiver Magnetron Case .....	5-40
Figure 5-8: Comparison of Pulse Pair and FFT Clutter Filters .....	5-64
Figure 5-9: FFT Processing — 50 pulse example .....	5-66
Figure 5-10: Effect of Windowing on FFT Response to Ground Clutter .....	5-67
Figure 5-11: Example of Fixed-Width Frequency Domain Clutter Filter .....	5-69
Figure 5-12: Example of Variable Width Frequency Domain Clutter Filter .....	5-70
Figure 5-13: Random Phase Processing Algorithm .....	5-76
Figure A-1: 40 dB IIR Clutter Filter Responses .....	A-3
Figure A-2: 50 dB IIR Clutter Filters Responses .....	A-4
Figure C-1: RVP7 Main Chassis .....	C-4
Figure C-2: RVP7 Main Chassis Back Panel .....	C-5
Figure C-3: Right, Left and Bottom View of RVP7 IFD Module .....	C-6
Figure C-4: Front View of RVP7 IFD Module .....	C-7
Figure C-5: View of RVP7 DAFC Module .....	C-8
Figure C-6: Right-side View of RVP7 Main Chassis .....	C-9
Figure C-7: Front, Top View of RVP7 Main Chassis .....	C-10

## Tables

Table 1-1: Examples of Dual PRF Velocity Unfolding .....	1-15
Table 2-1: Differences Among Versions of the IFD .....	2-1
Table 2-2: IFD Toggle Switch Settings .....	2-10
Table 2-3: IFD LED Indicator Interpretations .....	2-11
Table 2-4: IFD Internal Jumper Settings .....	2-11
Table 2-5: MMJ Connector P7 Pin Assignments .....	2-23
Table 2-6: SCSI Interface, DIN Connector Pin Assignments .....	2-24
Table 2-7: RVP7/AUX Board DIN Connector Pin Assignments .....	2-25
Table 2-8: DAFC Protocol Jumper Selections .....	2-27
Table 2-9: Pinout for the CTI "MVSR-xxx" STALO .....	2-29
Table 2-10: Bit Assignments for the IFD Coax Uplink .....	2-32
Table 5-1: Algebraic Quantities Within the RVP7 Processor .....	5-2
Table 5-2: Algorithm Results for +16dB Interference .....	5-8
Table 5-3: Algorithm Results for +26dB Interference .....	5-9
Table 6-2: RVP7 Status Output Words .....	6-22
Table A-1: Doppler 40dB Clutter Filter Coefficients .....	A-1
Table A-2: Doppler 50dB Clutter Filter Coefficients .....	A-2
Table C-1: Front Panel LED Indicator Interpretations .....	C-2
Table C-2: Summary of 25-Pin D Connectors .....	C-2
Table C-3: J10 & J11 TAG Lines, Pin Assignments .....	C-11
Table C-4: MISC I/O Connector, Pin Assignments .....	C-12
Table C-5: J13 Display Connector, Pin Assignments .....	C-13
Table C-6: BNC Connector Pin Assignments .....	C-14
Table C-7: J1 SCSI Connector Pin Assignments .....	C-15