C. Packaging

The complete RVP7 processor consists of two separate units connected by up to 100-meters of coax and fiber cables. The RVP7/IFD receiver module resides in the radar cabinet, while the main chassis is located near the host computer.

Both units feature universal input power supplies which sense the line voltage and automatically adjust without tap changes (100 – 240V AC 50 – 60 HZ). Consult the factory for operation on voltages outside of the specified ranges.

Important: Turn off power to the main chassis before installing or removing the PC board. The line cord should be disconnected before opening either the IFD module or main chassis.

The circuit boards contain many static sensitive components. Do not handle the boards or open the RVP7/IFD module unless a properly grounded wrist strap is worn.

C.1 Main Chassis General Description

SIGMET's main chassis is a 3-board rackmount/table top enclosure (17"W x 19.5"L x 5.25"H) (432 x 495 x 134mm) which fits a standard 19-inch EIA rack. The packaging is inherently expandable allowing the user the capability to upgrade from a basic single-board RVP7/Main by simply plugging in an additional one or two RVP7/AUX auxiliary processor boards. A perspective sketch of the chassis is shown in Figure C–1. A snap-off front panel allows the user easy access to the board for configuration and maintenance. A special 9U X 280 extender card can also be inserted.

Two fans mounted on the side of the enclosure draw ambient air through slots in the front, side and bottom. Do not block the slots or the exhaust grills on the fans. Check airflow now and then, and also check the board and slots for dust accumulation. If necessary, excessive dust accumulations on the board can be cleaned at a properly equipped static-free workstation with "canned air" or Chemtronics TF-Plus solvent, which can be purchased through electronics distributors.

The boards should be removed from the chassis and placed in their own protective cartons whenever the unit is shipped. Save the original packing provided for shipment.

A table top unit can be converted for rack mount by simply installing rack mount ears and removing the four rubber feet. The rack ears are installed with #8-32 flat head screws by first removing the small round caps and washers near the front on each side of the chassis. It is strongly recommended that the rack mount brackets supplied with the unit should be installed in the rack for additional structural support.

C.2 Main Chassis Front Panel

The front panel snaps off by applying downward and outward pressure to the top edge, exposing the board(s) and the front panel LED connection. The front panel can be detached from the LED cable by depressing the latch on the connector.

The three LEDs on the front panel are described in Table C–1.

Table C–1: Front Panel LED Indicator Interpretations

LED Label	Color	Function
POWER	Green	Verifies +5 output of the power supply.
GO	Green	Indicates power-up tests are passed.
USER	Red	Lighted via a special interface command from the host computer. Can also serve as a "busy" indicator.

The GO LED reports the final result of the self tests, so that proper functioning of the RVP7/Main and RVP7/AUX board(s) can be verified in the absence of a host computer. The USER LED can be controlled by the host computer, or it can be setup to indicate when each ray of data is being processed.

C.3 Main Chassis Back Panel

Figure C–2 shows the main chassis back panel. This panel handles the I/O to the radar, the RVP7/IFD module, and the host computer.

The back panel is equipped with a modular power entry device containing a line filter, switch, and fuse holder. For continued protection against risk of fire, replace only with same type and rating of fuse as marked on the back panel. The fuse may be accessed by first removing the line cord and opening the cover to the fuse compartment at the top with a small screwdriver.

The communication with the RVP7/IFD module is accomplished with two signals: The fiber-optic cable input called "FIBER-IN" and the BNC output signal on J16 labeled "UPLINK". The input contains high speed samples of the IF signal. It is directly connected to the fiber-optic input on the RVP7/Main board. The UPLINK signal contains control information for the RVP7/IFD module, such as burst pulse timing and AFC feedback.

The female 25-pin "D" connectors' pin assignments as installed by SIGMET are specified in the sheets that follow. The "D" connectors are summarized below. See Chapter 2 for a description of the signal meanings.

Table C–2: Summary of 25-Pin D Connectors

Label	Function
J10 "TAG 0-15"	16-bit AZ angle input option, see Table C–3
J11 "TAG 16-31"	16-bit EL angle input option, see Table C–3
J12 "MISC I/O"	Pulse width control, polarization control, end of ray strobe, see Table C–4
J13 "DISPLAY"	Serial line for real-time display or angle info, see Table C–5

The 11 BNC's (plus 4 spares) are used for 75 ohm coax I/O and are labeled as shown on Figure C–2. The wiring between these connectors and the RVP7 board is described in Table C–6. The I-OUT, Q, LOG BNC's are for the in-phase, quadrature, and LOG receiver video outputs from the radar receiver.

J20 through J25 are the 6 trigger outputs. The timing of these triggers is configured by the user using the TTY setup (see section 3.3.5). They are usually configured to be driven by 75-ohm coax drivers. They can optionally be TTL level signals. For the first three this is selected by on-board jumpers (see section 2.2.7), the last three can be changed using wirewrapping on the backplane. The TR-IN (J19) is used if the trigger source is external to the RVP7. Usually, however, the RVP7 is used to generate the trigger. This feature is selected using the TTY setup (see section 3.3.4).

The right side of the back panel contains the SCSI interface to the host computer on connector J1. The pinout of this connector is described in Table C–7. Inside the chassis, connections are made via a flat 96-pin cable.

C.4 RVP7/IFD Module General Description

The RVP7/IFD module is a small metal box which can be mounted inside the receiver cabinet. A perspective sketch of the module is shown in the attached Figure. Cooling of the inside components is accomplished by direct conduction to the case. It is desirable to place the module in an environment that allows external convective cooling.

Figure C–1: RVP7 Main Chassis

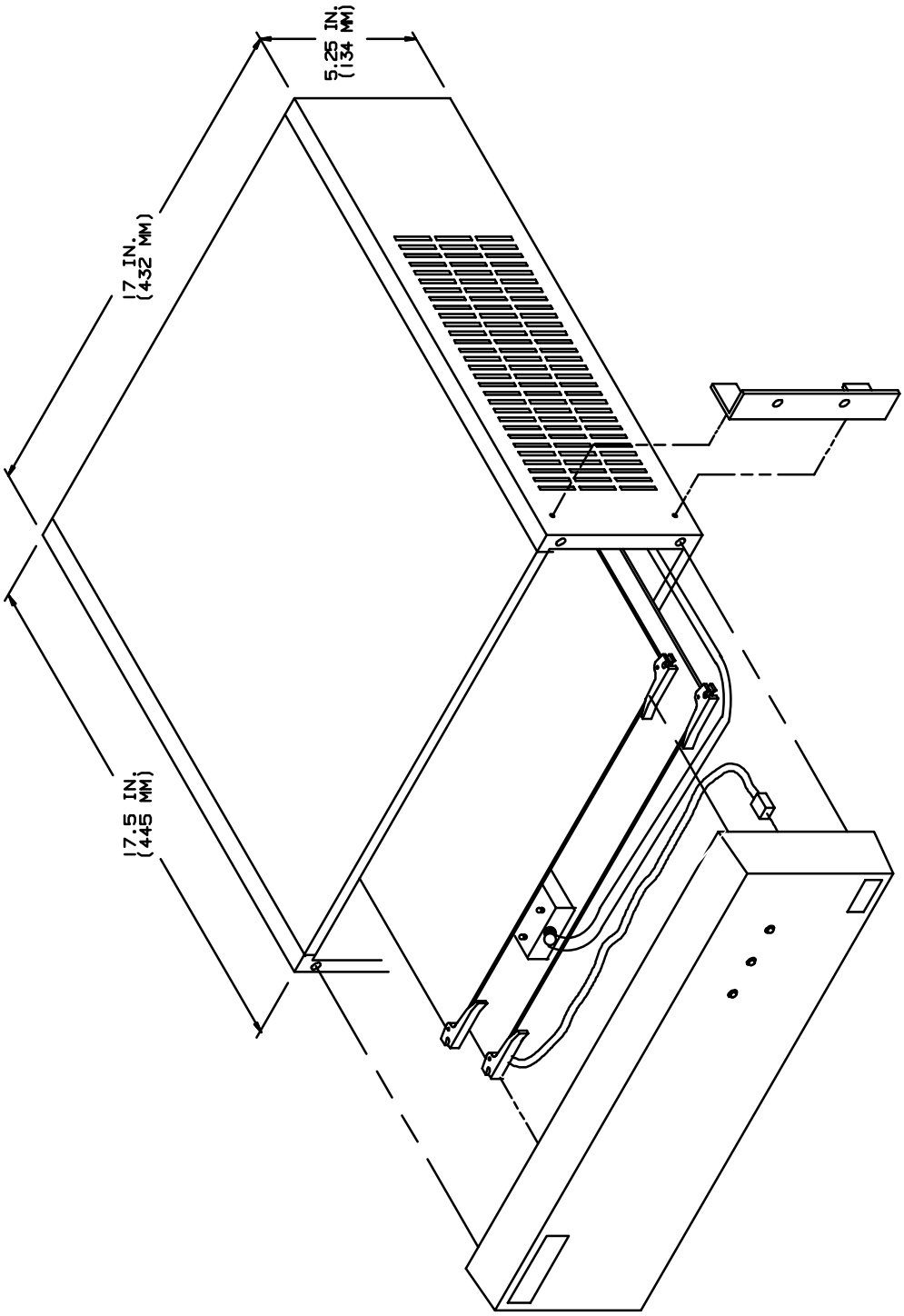

Figure C–2: RVP7 Main Chassis Back Panel

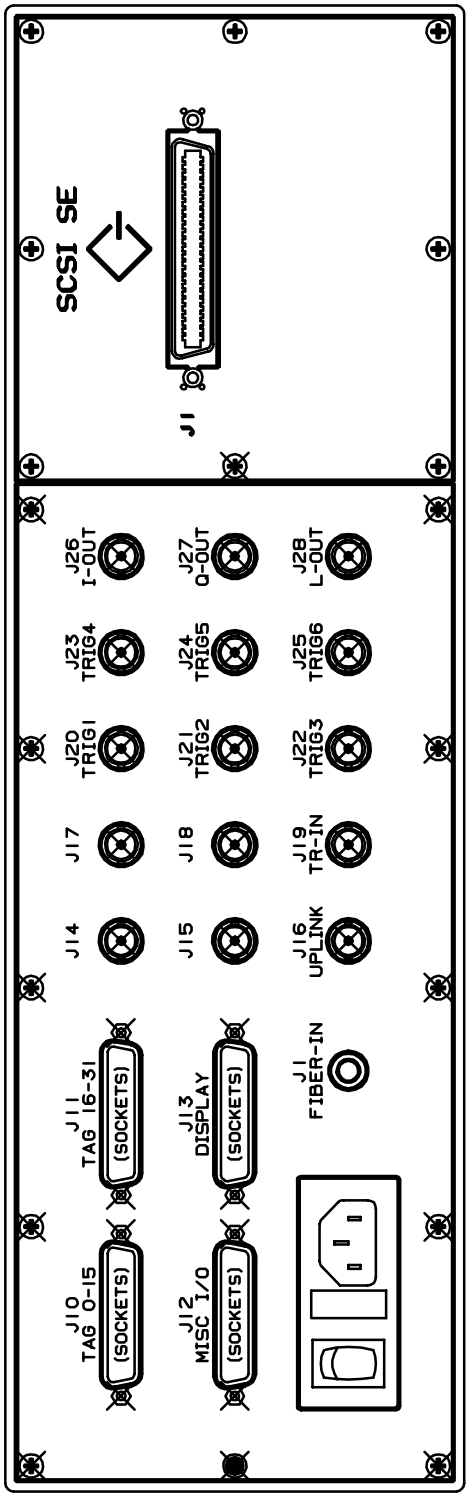

Figure C–3: Right, Left and Bottom View of RVP7 IFD Module

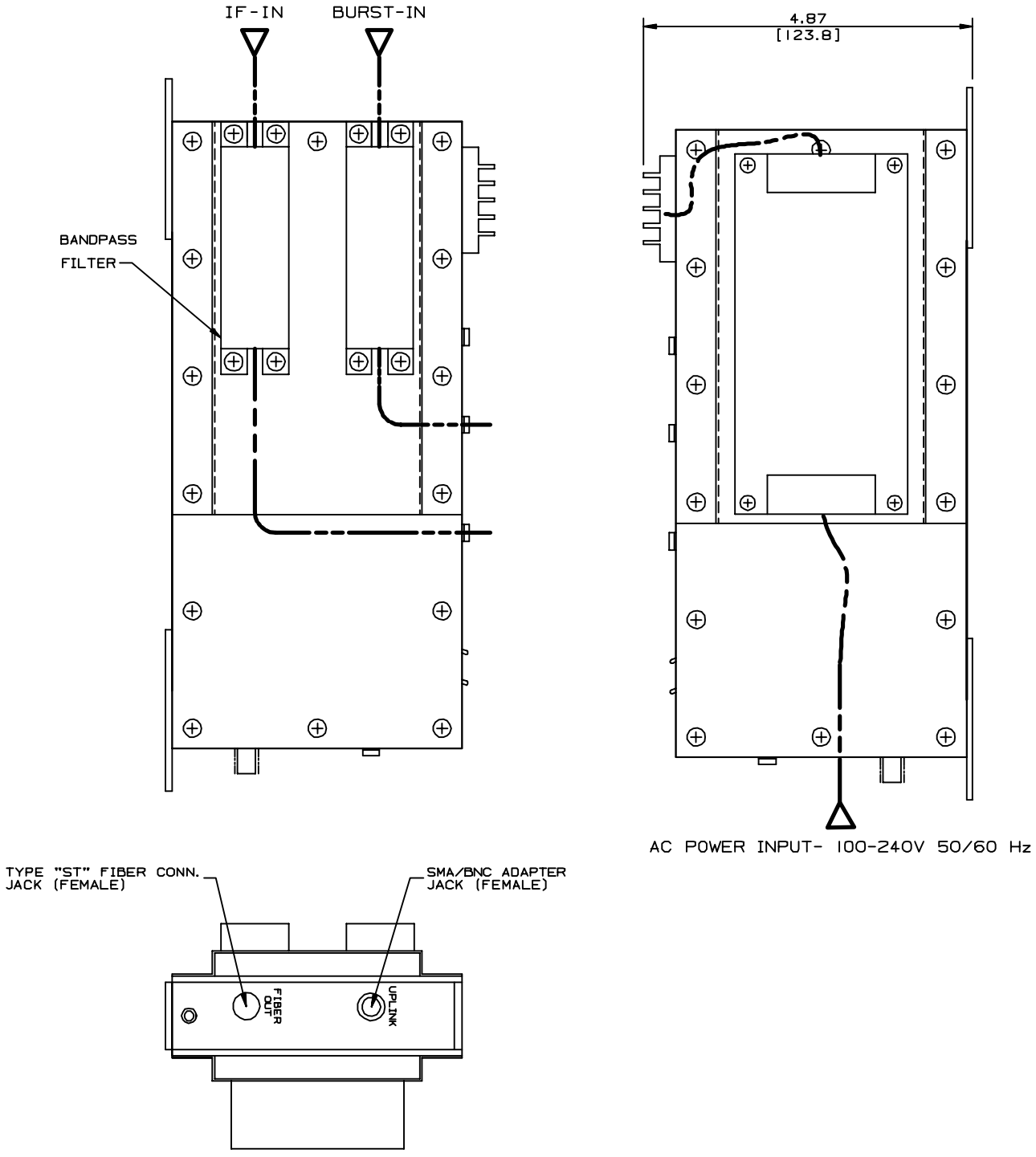

Figure C–4: Front View of RVP7 IFD Module

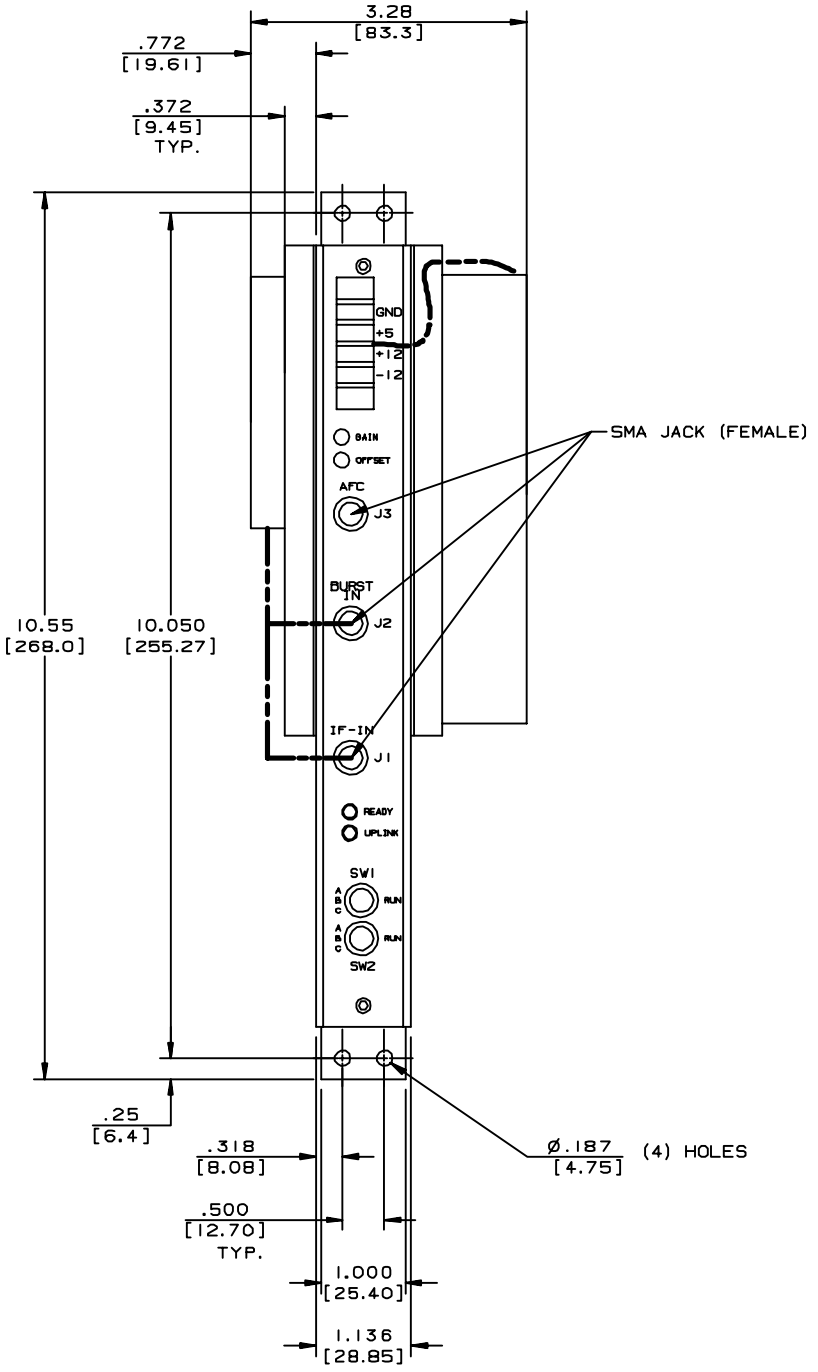

Figure C–5: View of RVP7 DAFC Module

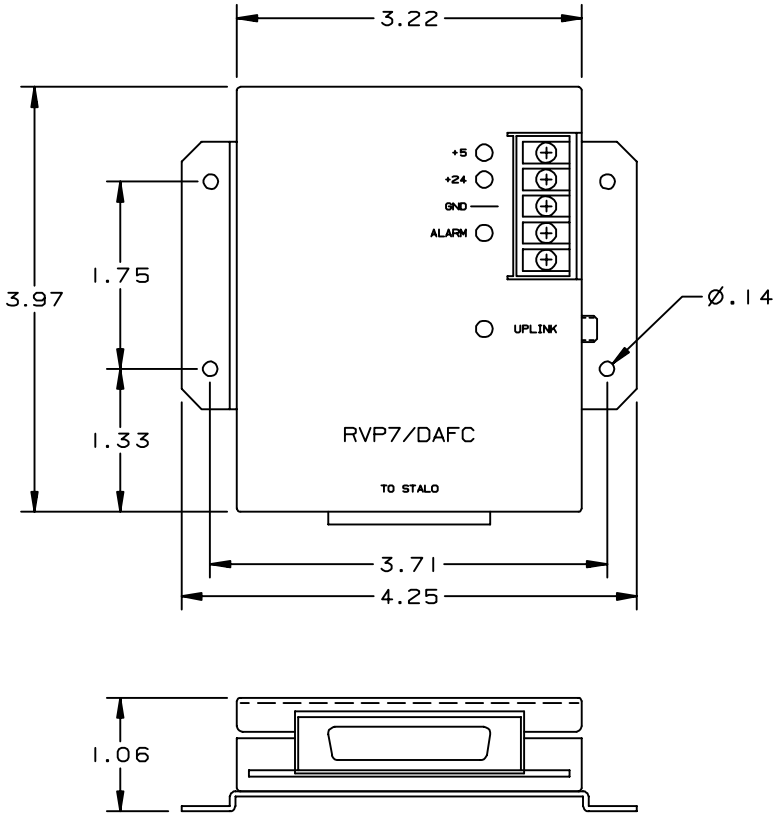

Figure C–6: Right-side View of RVP7 Main Chassis

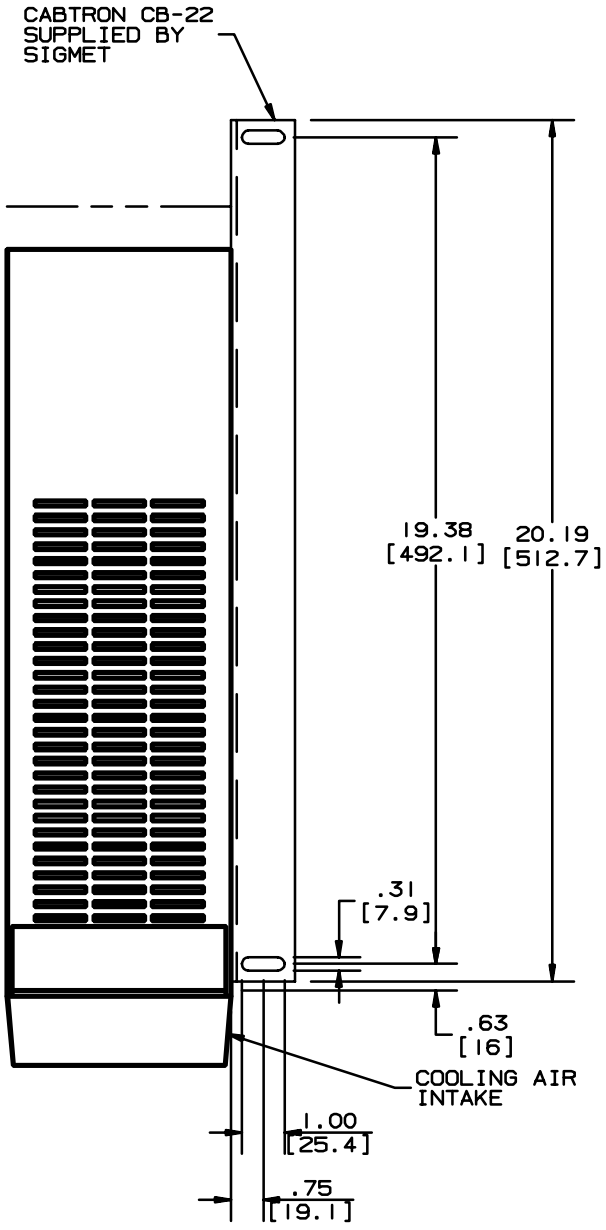

Figure C–7: Front, Top View of RVP7 Main Chassis

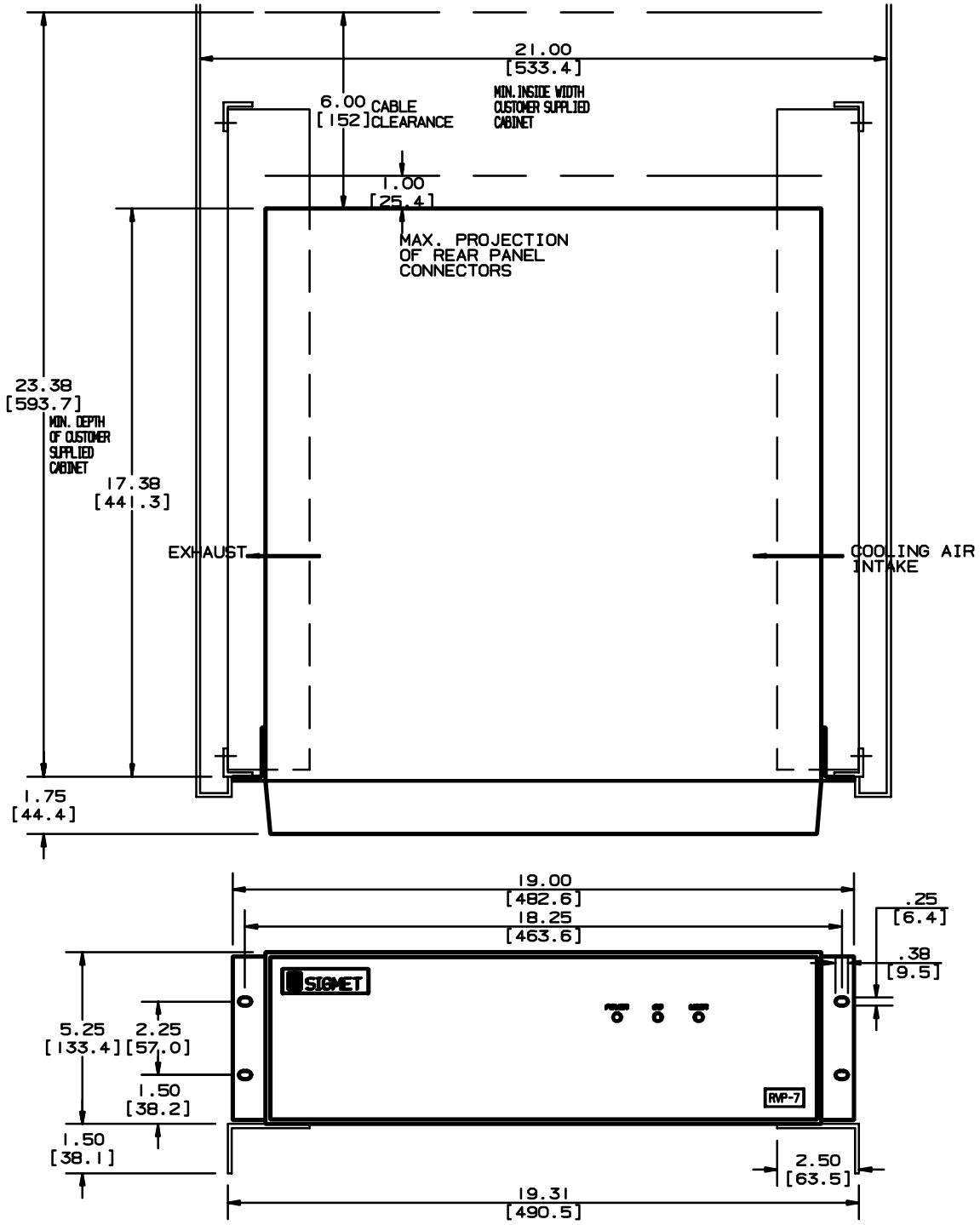

Table C–3: J10 & J11 TAG Lines, Pin Assignments

Panel J10	Signal Name	B'plane P1J3	50-pin Ribbon	Panel J11	Signal Name	B'plane P1J3	50-pin Ribbon
1	TAG0	A3	25	1	TAG16	C3	50
2	TAG1	A4	23	2	TAG17	C4	48
3	TAG2	A5	21	3	TAG18	C5	46
4	TAG3	A6	19	4	TAG19	C6	44
5	TAG4	A7	17	5	TAG20	C7	42
6	TAG5	A8	15	6	TAG21	C8	40
7	TAG6	A9	13	7	TAG22	C9	38
8	TAG7	A10	11	8	TAG23	C10	36
9	TAG8	A11	9	9	TAG24	C11	34
10	TAG9	A12	7	10	TAG25	C12	32
11	TAG10	A13	5	11	TAG26	C13	30
12	TAG11	A14	3	12	TAG27	C14	28
13	TAG12	A15	1	13	TAG28	C15	26
14	TAG13	A16	24	14	TAG29	C16	49
15	TAG14	A17	22	15	TAG30	C17	47
16	TAG15	A18	20	16	TAG31	C18	45
17	—		18	17	—		43
18	—		16	18	—		41
19	—		14	19	—		39
20	—		12	20	—		37
21	—		10	21	—		35
22	—		8	22	—		33
23	GND	B3	6	23	GND	B6	31
24	GND	B4	4	24	GND	B7	29
25	GND	B5	2	25	GND	B8	27

Table C–4: MISC I/O Connector, Pin Assignments

Panel J12	Signal Name	B'plane P1J2	50-pin Ribbon
1	—		25
2	PWBW0	A15	23
3	PWBW1	A16	21
4	PWBW2	A17	19
5	PWBW3	A18	17
6	—		15
7	—		13
8	—		11
9	—		9
10	GND	B15	7
11	GND	B21	5
12	GND	B20	3
13	GND	B16	1
14	—		24
15	POLAR0	A13	22
16	POLAR1	A14	20
17	SCLK_	C17	18
18	ENDRAY_	C18	16
19	—		14
20	—		12
21	—		10
22	—		8
23	GND	B18	6
24	GND	B17	4
25	GND	B19	2

Table C–5: J13 Display Connector, Pin Assignments

Panel J13	Signal Name	B'plane P1J1	50-pin Ribbon
1	FGND	Jmp to Chassis	50
2	SIORCV	B27	48
3	SIOXMT	B28	46
4	SIORTS	B29	44
5	SIOCTS	B30	42
6	—		40
7	DCGND	A32	38
8	—		36
9	—		34
10	PH7–	C18	32
11	PH6–	C16	30
12	PH5–	C14	28
13	PH4–	C12	26
14	PH3–	C10	49
15	PH2–	C8	47
16	PH1–	C6	45
17	PH0–	C4	43
18	PH7+	C17	41
19	PH6+	C15	39
20	PH5+	C13	37
21	PH4+	C11	35
22	PH3+	C9	33
23	PH2+	C7	31
24	PH1+	C5	29
25	PH0+	C3	27

Note: The phase control outputs are optional, not wired on all chasses. They can also be used for digital AFC output. Note that the main board jumpers JP23 and JP24 must be in the AB position for the upper two control lines to be driven.

Table C–6: BNC Connector Pin Assignments

Back Panel		Conductor-Connection			Shield-Connection		
#	**Label**	**Signal**	**J2**	**50-pin Ribbon**	**Signal**	**J2**	**50-pin Ribbon**
J14				7			8
J15				4			5
J16	"UPLINK"	UPLINK	C14	1	GND	B14	2
J17				16			17
J18				13			14
J19	"TR–IN"	TRIGIN	C13	10	GND	B13	11
J20	"TRIG1"	TGEN0	A19	25	GND	B19	26
J21	"TRIG2"	TGEN1	A20	22	GND	B20	23
J22	"TRIG3"	TGEN2	A21	19	GND	B21	20
J23	"TRIG4"	A75OUT	C22	34	GND	B19	35
J24	"TRIG5"	B75OUT	C23	31	GND	B20	32
J25	"TRIG6"	C75OUT	C24	28	GND	B21	29
J26	"I–OUT"	IVID+	B5	43	IVID–	C5	44
J27	"Q–OUT"	QVID+	B7	40	QVID–	C7	41
J28	"L–OUT"	LVID+	B9	37	LVID–	C9	38

Note: TGEN3, TGEN4 and TGEN5 have been connected to the back panel via the 75-ohm coax signal drivers. These are wire-wrapped on the backplane center DIN connector P1J2 attached to P2 of the RVP7/main board. The wiring is as follows:

TGEN3	C19	TO	A75IN	A22	BLUE
TGEN4	C20	TO	B75IN	A23	BLUE
TGEN5	C21	TO	C75IN	A24	BLUE

Table C–7: J1 SCSI Connector Pin Assignments

Signal Name	Connector Contact #	Signal Name	Connector Contact #
GROUND	1	–DB (0)	2
GROUND	3	–DB (1)	4
GROUND	5	–DB (2)	6
GROUND	7	–DB (3)	8
GROUND	9	–DB (4)	10
GROUND	11	–DB (5)	12
GROUND	13	–DB (6)	14
GROUND	15	–DB (7)	16
GROUND	17	–DB (P)	18
GROUND	19	GROUND	20
GROUND	21	GROUND	22
RESERVED	23	RESERVED	24
OPEN	25	TERMPOWER	26
RESERVED	27	RESERVED	28
GROUND	29	GROUND	30
GROUND	31	–ATN	32
GROUND	33	GROUND	34
GROUND	35	–BSY	36
GROUND	37	–ACK	38
GROUND	39	–RST	40
GROUND	41	–MSG	42
GROUND	43	–SEL	44
GROUND	45	–C/D	46
GROUND	47	–REQ	48
GROUND	49	–I/O	50