2. Hardware Installation

This chapter describes how to install the RVP7 hardware. Topics include mechanical installation and siting, electrical specifications of the interface signals, system-level considerations, chassis connector assignments, and jumper settings.

2.1 IFD IF Digitizer Module

The IFD IF digitizer is housed in an electrically sealed solid metal enclosure to achieve good immunity to external electrical noise. The internal circuitry has been designed to minimize the number of digital components, and it is carefully grounded and shielded to make the cleanest possible samples of the input IF signal. The unit is cooled by direct conduction of heat through the metal chassis; there are no openings required for airflow.

There have been several versions and evolutions of the IFD. The main text of this manual describes the current hardware version, which is the 14-bit Rev.D circuit board. Table 2–1 summarizes the differences among all of the versions that have been manufactured so far.

Table 2–1: Differences Among Versions of the IFD

	Rev.B	***Rev.C***	***Rev.D***
A/D Chip	Analog Devices AD9042, 12–Bits		AD6644, 14–Bits
Input Signal Level	A/D saturation at +4.5dBm		A/D saturation at +6.0dBm
A/D Noise Density	–76dBm/MHz		–82dBm/MHz
Dynamic Range	93dB at 0.5MHz		101dB at 0.5MHz
Ext-Clock	No	Yes (shared with AFC connector)	
Noise Generator	None. The A/D dither power must be supplied from wideband thermal noise in the RF/IF chain.		Built-in noise source supplies A/D dither power in the 200–900KHz range.
Power Supplies	+5V, +12V, –12V		+5V Only. ±12/15V required only for analog AFC output
Jumpers (Table 2–4)	None	AFC/Clock I/O	AFC/Clock I/O Dither and Config Selections
Uplink Protocols	AFC-16	AFC-16 & PLL-16	Supports full set of protocols defined in Section 2.5.1
First Production	March 1997	April 1998	December 2000

The IFD module takes the place of many individual components that are found in a traditional analog radar receiver:

- LOG Receiver
- Quad Phase Detector
- Linear Amplifier and AGC circuitry
- IF Band Pass Filters
- COHO and associated locking circuitry
- AFC feedback circuit

2.1.1 Input A/D Saturation Levels

There are two analog signals that must be supplied to the IFD:

- IF receiver signal
- IF Burst Pulse for magnetron, or COHO reference for klystron.

Both of these inputs are on SMA connectors. The IF signal should be driven by the front-end mixer/LNA/IF-Amp. components, similar to the way that a LOG receiver would normally be installed. The magnetron burst pulse or klystron COHO reference is also derived in the same manner as a traditional analog receiver.

The A/D input saturation level for both the IF-Input and Burst-Input is +6 dBm (4.5 dBm for Rev.C or earlier). In almost all installations an external anti-alias filter is installed on both of these inputs. These filters (if supplied by SIGMET) are mounted externally on one side of the IFD, and have an insertion loss of approximately 1–2dB. Thus, the input saturation level will be +8dBm measured at the filter inputs.

For the burst pulse or COHO reference it is important not to exceed the A/D saturation level. This reference signal should be strong enough so that most of the bits in the A/D converter are used effectively, but it should also allow a few deciBels below the saturation level for safety. The recommended power level is in the range +1 to –12 dBm, measured as described in section E.16. This is important for making a precise phase measurement on each pulse.

In contrast, for the IF receiver input it is permissible (in fact desirable) to occasionally exceed the A/D input saturation level at the strongest targets. The RVP7 employs a statistical linearization algorithm to derive correct power levels from targets that are as much as 6dB above saturation. The actual IF signal level should be established by weak-signal and noise considerations (see below), rather than by working backwards from the saturation level.

2.1.2 IF Bandwidth and Dynamic Range

The RVP7 performs best with a wide bandwidth IF input signal. This is because a wideband signal can be made free of phase distortions within the (relatively narrow) matched passband of the received signal. The RVP7 uses an external analog anti-aliasing filter at each of its IF and

Burst inputs. The purpose of these filters is to block frequencies that would otherwise alias into the matched filter passband. The anti-alias filters have a nominal passband width of 14 MHz centered at 30MHz, i.e. from 23MHz to 37MHz. This is the recommended operating bandwidth for the IF signal, although the RVP7 will still work successfully with lesser IF bandwidth.

At the 36MHz sampling rate the quantization noise introduced by LSB uncertainties is spread over an 18MHz bandwidth. For an ideal 14-bit A/D converter that saturates at +6dBm the effective quantization noise level would be:

$$+6dBm - 20log(2^{14}) - 10log(\frac{18MHz}{1MHz}) \quad = \quad -90\frac{dBm}{MHz}$$

If samples from this ideal converter were processed with a digital filter having a bandwidth of 1MHz, then an input signal at –90dBm would have a signal-to-noise ratio of 0dB. A narrower FIR passband (corresponding to a longer transmitted pulse) would decrease the quantization noise even further, so that 0dB SNR would be achieved at even lower input power.

In practice, the 14-bit A/D converter used inside the IFD does not behave quite this well. The Analog Devices AD6644 chip has been measured to have a wideband SNR of 76dB, i.e., 8dB less than the 84dB range expected for an ideal converter. The above calculation for noise density thus becomes:

$$+6dBm - 76dB - 10log(\frac{18MHz}{1MHz}) \quad = \quad -82\frac{dBm}{MHz}$$

Indeed, the RVP7's receiver power monitor described in Section 4.6 will show a filtered power level of approximately –82dBm when the FIR bandwidth is 1MHz and the IFD inputs are terminated in 50–Ohms.

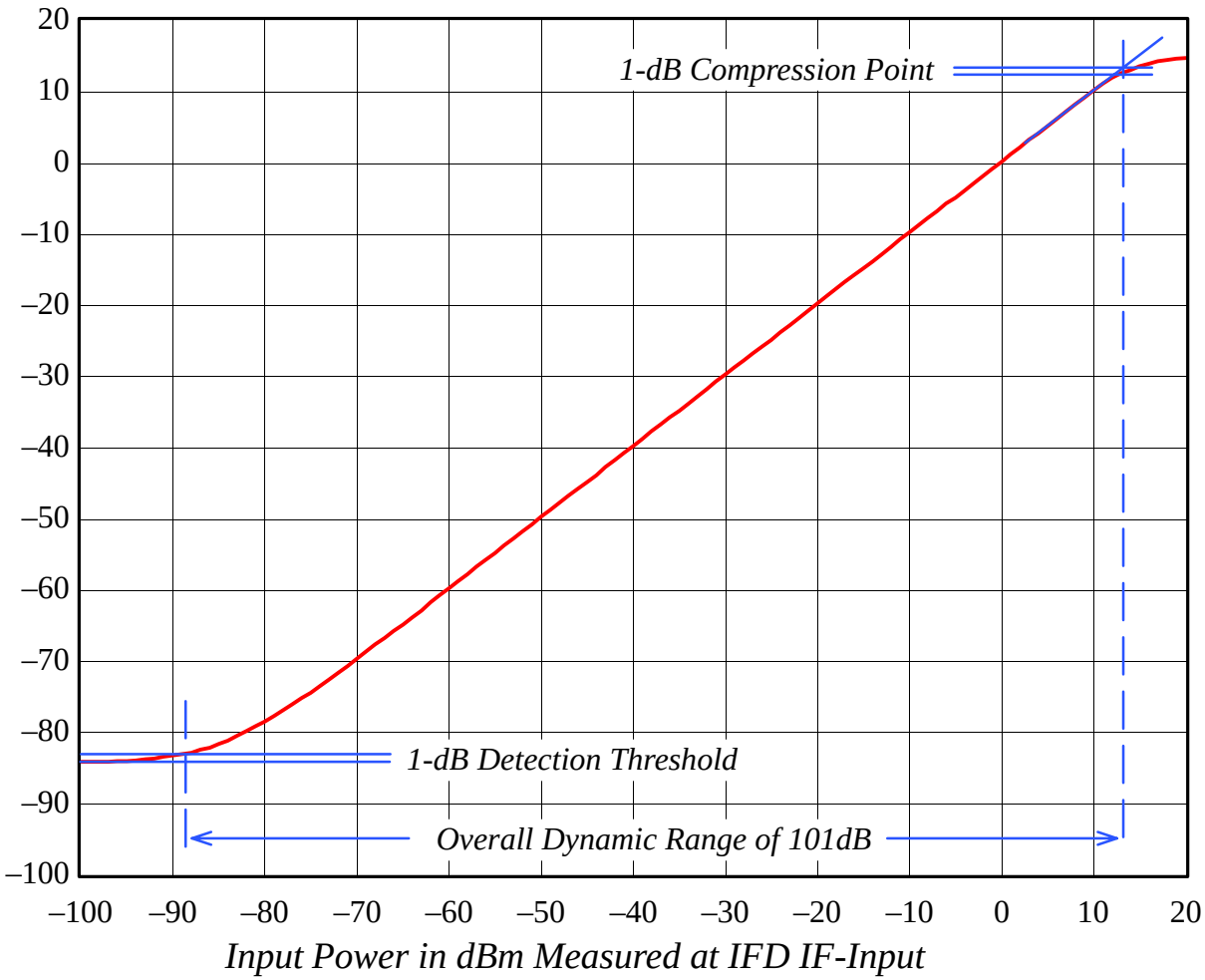
The inverse correspondence between filter bandwidth and the 0dB SNR signal level leads to an interesting and useful property of wideband digital receivers: they can operate over a dynamic range that is much greater than the inherent SNR of their A/D converter would imply. If this particular A/D chip were performing direct conversion at "base band" it would have a dynamic range of only 76dB. However, by utilizing the extra bandwidth of the converter, the RVP7 is able to extend the dynamic range to approximately 100dB.

To understand this, begin with the 88dB interval between the converter's +6dBm saturation level and the –82dBm 0dB SNR level at 1MHz bandwidth. Add to this:

- 6dB for the statistical linearization that is performed on signals that exceed the saturation level. The RVP7 can recover signal power accurately even when the A/D converter is driven beyond saturation. Velocity data will also be valid, but spectral width may be overestimated.
- 4dB for usable dynamic range below the 0dB SNR level. In practice, a coherent signal at –4dB SNR can easily be measured when 25 or more pulses are used.

Thus, the overall dynamic range at 1MHz bandwidth (approx. 1 μsec transmit pulse) is 88+6+4 = 98dB. For a 0.5 μsec pulse the dynamic range would be reduced to 95dB; but it would increase to 101dB for a 2.0 μsec pulse. An actual calibration curve demonstrating this performance is shown in Figure 2–1, for which the RVP7's digital bandwidth was set to 0.53MHz and external signal generator steps of 1dB were used over the full operating range.

Figure 2–1: Calibration Plot for a Stand-alone 14-Bit IFD

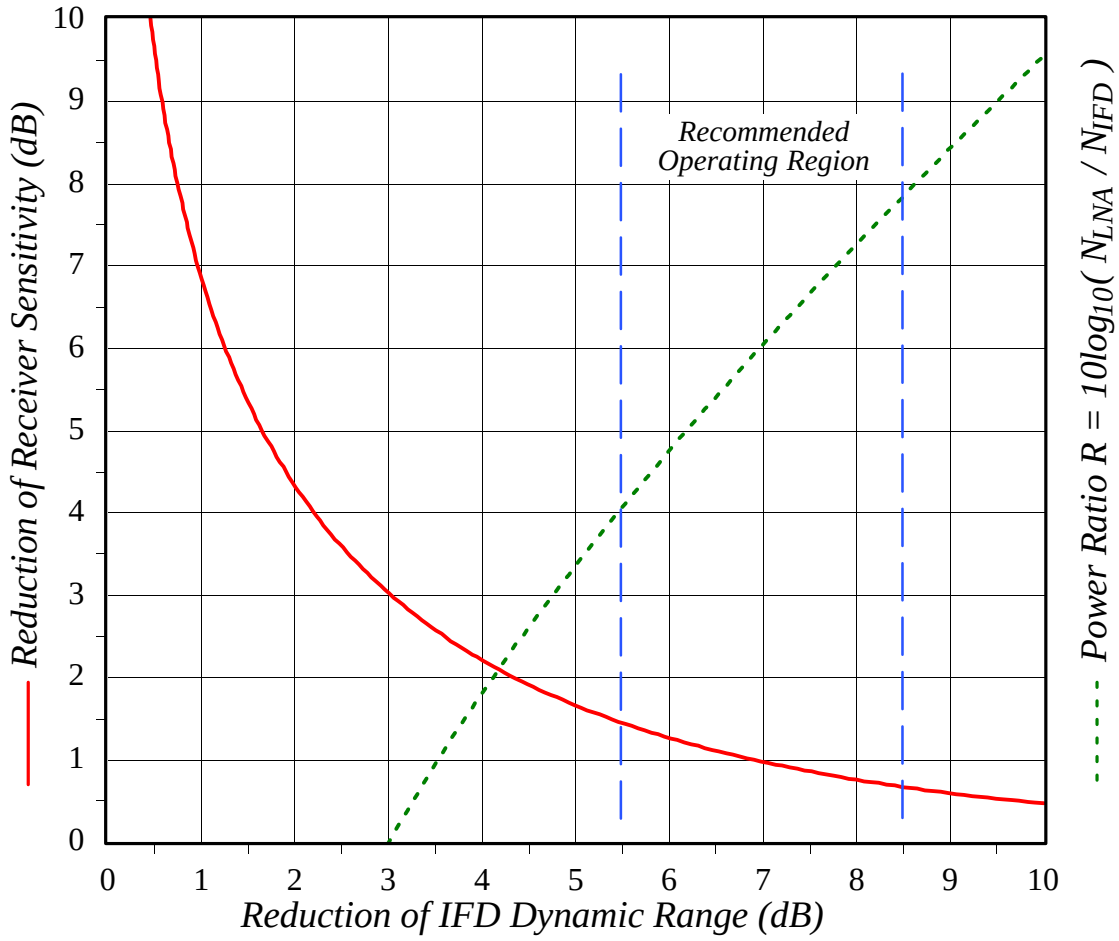


2.1.3 IF Gain and System Performance

The previous discussion was concerned with measuring the dynamic range of a stand-alone IFD. We will now examine how the unit performs in the context of a complete radar receiver. We assume that an LNA/Mixer has already been selected that offers an appropriate balance between price and noise figure. Having chosen these front-end components, the only parameter that remains to be determined is the total RF/IF gain between the antenna waveguide and the IFD.

Assume that the thermal noise *(kT)* of the system is –114dBm/MHz, and that the noise figure of the LNA/Mixer is 2dB. We wish to bring this –112dBm/MHz noise level up into the working range of the IFD so that the received echoes can be optimally processed. However, in trying to select the required gain, we realize that we must make a tradeoff between preserving the receiver sensitivity that has been established by the LNA, and preserving the overall dynamic range of the IFD. This is the exact same tradeoff that is made in traditional multi-stage analog receiver systems that include a wide dynamic range LOG receiver.

Figure 2–2: Tradeoff Between Dynamic Range and Sensitivity



The solid red curve in Figure 2–2 shows that these two variables interact in a symmetric manner, so that any operating point *(x,y)* is always matched by a dual operating point at *(y,x)*. To understand the construction of this plot, let N_{IFD} represent the stand-alone (terminated input) noise power of the IFD over some bandwidth. Similarly, let N_{LNA} represent the LNA/Mixer thermal noise power over that same bandwidth, and after amplification by all RF and IF stages. Note that N_{IFD} is primarily due to the quantization noise that is introduced by the A/D converter, whereas N_{LNA} has its origins in the fundamental thermal noise of the receiving system. The reduction of receiver sensitivity is the amount by which the LNA thermal noise is increased over the original level established by the front-end components:

$$\Delta Sensitivity = 10\log_{10}(N_{LNA} + N_{IFD}) - 10\log_{10}(N_{LNA}) = 10\log_{10}\left(1 + \frac{N_{IFD}}{N_{LNA}}\right)$$

Likewise, the reduction of RVP7 dynamic range is the amount by which the IFD quantization noise is increased over its stand-alone value:

$$\Delta DynamicRange = 10\log_{10}(N_{LNA} + N_{IFD}) - 10\log_{10}(N_{IFD}) = 10\log_{10}\left(1 + \frac{N_{LNA}}{N_{IFD}}\right)$$

Note that both of these quantities depend only on the ratio of the two powers; hence, the two equations define a parametric relationship in the dimensionless variable $R = (N_{LNA} / N_{IFD})$. Figure 2–2 was created by sweeping the value of *R* from 1/9 to 9. The solid red curve shows the locus of ($\Delta DynamicRange$, $\Delta Sensitivity$) points, and the dashed green curve shows *R* itself (expressed in dB) as a function of $\Delta DynamicRange$. For example, when the LNA noise power is equal to the IFD noise power, *R* is 1.0 (0dB) and there will be a 3dB reduction in both sensitivity and dynamic range.

The recommended operating region is the portion of the curve that limits the loss of sensitivity to between 1.4dB and 0.65dB. The attendant loss of dynamic range will fall between 5.5dB and 8.5dB respectively. Each axis of the plot has an important physical interpretation within the radar system.

- The horizontal axis is equivalent to the increase in the RVP7's report of filtered power when the IF-Input coax cable is connected versus disconnected. This is an easy quantity to measure, and thus provides a simple way to check the overall gain of the LNA/Mixer/IF components.
- The vertical axis is equivalent to a worsening of the LNA/Mixer noise figure. This can also be interpreted as the amount of transmit power that is, in some sense, "wasted" when observing very weak echoes. If you have installed an expensive LNA with a very low noise figure, then you will want to pick an operating point that makes the most of preserving that investment.

Figure 2–2 can be used to calculate the net gain that is required by the front-end components, and to predict the final system performance:

1. Choose an operating point that balances your need for sensitivity versus dynamic range. For this example, we will allow a 1dB loss of sensitivity from the theoretical limit of the LNA/Mixer, and will assume a bandwidth of 0.5MHz.
2. For a 1dB loss of sensitivity, the $\Delta DynamicRange$ is first determined from the solid red curve as 7dB. The required noise ratio *R* is then read vertically on the dashed green curve as 6.1dB.
3. Thus, the RF/IF gain must bring the front-end thermal noise at –112dBm/MHz up to a level that is 6.1dB higher than the IFD noise density of –82dBm/MHz. The gain is therefore (–82dBm/MHz + 6dB) – (–112dBm/MHz) = 36dB. Note that this gain does not depend on bandwidth, and therefore will be correct for all pulsewidth/bandwidth combinations.
4. The dynamic range for the complete system at 0.5MHz bandwidth may now be calculated as 101dB – 7dB = 94dB.
5. After assembling all of the RF and IF components we can check whether we achieved the correct gain by verifying a 7dB rise (independent of bandwidth) in RVP7 filtered power when the IF-Input cable is connected versus disconnected.

Keep in mind when designing your RF and IF components that the final amplifier driving the IFD must be capable of driving up to +14dBm, so that signals above saturation can be correctly measured.

2.1.4 Choice of Intermediate Frequency

The RVP7 does not assume any particular relationship between the A/D sample clock and the receiver's intermediate frequency. You may operate at any IF that is at least 4MHz away from any multiple of half the 35.9751MHz sampling rate. The valid frequency bands are thus: 22–32MHz, 40–50MHz or 58–68MHz. There are many reasons for staying clear of these Nyquist frequency multiples. Most of these considerations would apply to all types of digital processors, and are not specific to the RVP7.

As an example of what can go wrong at the Nyquist frequencies, suppose that an intermediate frequency of 35MHz was used. This is only 1MHz away from the (approximately) 36MHz sampling rate. The external anti-alias filter must now be designed much more carefully since a spurious input signal at 37MHz would be aliased into the valid 35MHz band. If the valid signal bandwidth were 2MHz, then the anti-alias filter would have the difficult task of passing 34–36MHz free of distortion while rejecting everything above 36MHz. The filter's transition zone would have to be very sharp, and this is difficult to achieve.

Another problem that would arise with a 35MHz IF on a magnetron system would be the RVP7's computation of AFC. If the processor can not distinguish 37MHz from 35MHz, then it can not tell the difference between the STALO being correctly on frequency, versus being 2MHz too high. The symmetric AFC tracking range would be reduced to the very small interval 34–36MHz.

For similar reasons (i.e., transition band width), the digital FIR filter itself also becomes difficult to design when its passband is near a Nyquist multiple. But there is an additional constraint that the digital filter should have a very large attenuation at DC. This is so that fixed offsets in the A/D converter do not propagate into the synthesized "I" and "Q" data. Since 36MHz is aliased into DC, we are left with the contradictory requirements of a zero very close to the edge of the filter's passband.

2.1.5 AFC Output Voltage (Optional)

An analog AFC voltage is produced by a 16-bit DAC whose output limits are –10V to +10V. Gain and Offset potentiometers on the IFD module set the actual operating span within these limits. Use the switch settings described below to force the low, center, and high voltages to be output, and then adjust the two potentiometers so that the desired voltage span is achieved. The Offset adjustment is independent of the Gain adjustment. Hence, a good strategy is to first set the switches for the midpoint voltage, and adjust the Offset potentiometer so that the center IF frequency is produced by the STALO mixer. Then, adjust the Gain potentiometer for the desired tuning range around that center point. The midpoint voltage will not change as you vary the overall span.

AFC voltage output is always enabled on Rev.B (and earlier) IFD boards. On Rev.C (and later) boards, the AFC function shares the same connector with the optional reference clock input (See Section 2.1.6). AFC can be enabled on a Rev.C board as follows:

- Remove U14
- Install U11, U12, U13

- Set JP1 to its AB position, which is also labeled "AFC".
- Install fixed frequency stable 35.975MHz oscillator at U5.

The instructions are similar for a Rev.D board except that you do not need to remove U14, and you must check that no jumper has been placed on JP3/BC.

Additional information about using AFC can be found in Sections 2.2.4, 2.4, 3.3.6, and 5.1.2.

2.1.6 Reference Clock Input (Optional)

When the RVP7 is used in a klystron system, or in any type of synchronous radar, the radar COHO is supplied to the IFD so that the processor can digitally lock to it. The COHO phase is measured at the beginning of each transmitted pulse, and is used to lock the subsequent (I,Q) data for that pulse. The COHO phase is measured relative to the IFD's own internal stable sampling clock, which is nominally 35.975MHz. The internal sampling clock itself is not affected by the application of the COHO. Rather, A/D samples of the COHO are obtained at the fixed sampling rate, and the (I,Q) data are digitally locked downstream in the RVP7/Main processing chain. The procedure is identical to the manner in which phase is recovered in a magnetron system, except that the COHO signal is used in place of a sample of the transmit burst.

There are two special concerns that may come up when the RVP7 is used in the above manner within a synchronous radar system. Both concerns are the result of the IFD's sampling clock being asynchronous with the radar system clock.

- ***RVP7 Generates the Radar Trigger***
  The trigger signals supplied by the RVP7 are synchronous with the IFD data sampling clock. This is accomplished by a clock recovery PLL on the RVP7/Main that provides on-board timing which is identical to the sampling clock in the IFD. However, since the IFD sampling clock is asynchronous with the radar clock(s), the RVP7 trigger outputs are likewise asynchronous. The result is that each transmitted pulse envelope will be triggered independently of the COHO phase. The transmitted pulse is still synchronous — but the precise alignment of the amplitude modulated envelope will vary.

  In almost all cases, the exact placement of the transmitter's amplitude envelope does not affect the overall system stability, nor the ability of the RVP7 to reject ground clutter and to process multi-mode return signals. For this reason, a synchronous radar system that is triggered using the RVP7 triggers will still perform optimally using the standard digital COHO locking techniques. In spite of this, however, some system designers may still prefer that the amplitude envelope itself be locked to the COHO.

- ***RVP7 Receives the Existing Radar Trigger***
  When an external trigger is supplied to the RVP7, the processor synchronizes its internal range bin selection circuitry to that external trigger. The placement of the range bins themselves, however, is always synchronous with the IFD's

35.975MHz acquisition clock. The result is that 27.8ns of jitter is introduced in the placement of the RVP7's range bins relative to the transmitted pulse itself.

The effect of this synchronization jitter is that targets appear to be fluctuating in range by approximately 4.2 meters. Although this is small relative to the range bin spacing itself, and thus does not affect the range accuracy of the data, the effect on overall system stability is more severe. Using both numerical modeling and actual field measurements, we have found that sub-clutter visibility of a μsec pulse may be limited to approximately 43dB as a result of this 27.8ns range jitter. This falls quite short of the usual expectations of a synchronous radar system in which clutter rejection of 55–60dB should be attainable.

The solution to either of the above concerns is to provide some means for the IFD's internal sampling clock to be phase locked to the radar system. If the RVP7 provides the radar triggers, then those triggers would become synchronous with the radar COHO; and if the RVP7 receives an external trigger, then its range bin clock would be synchronous with that external trigger, and thus, there will be no synchronization jitter in the range bins.

The Rev. C version of the IFD offers the option of locking its sampling clock to an external system clock reference. This results in an RVP7 that is fully synchronous with the existing radar timing. Rather than being derived from a fixed-frequency oscillator, the phase locked IFD sampling clock is driven by a custom Voltage-Controlled-Crystal-Oscillator (VCXO). This oscillator can have a center frequency in the 33.5 to 39.5MHz range, which is any rational multiple P/Q of twice the input reference frequency, where P and Q are integers between 1 and 128 (See also, Section 3.3.6). The tuning range of the VCXO is purposely kept very narrow (to improve the clock stability), and is restricted to approximately +/–50ppm. Thus, the input reference clock frequency must be precisely specified so as to stay within these limits.

The reference clock input frequency range is 2–60 MHz, and the input power level level must be between –10 and 0dBm. Use the following configuration to allow a Rev.C IFD to lock its sampling clock to an external reference:

- Install U14
- Remove U11, U12, U13
- Set JP1 to its BC position to terminate the reference input in 50Ω, or leave the jumper open to achieve a high-impedance input (approx. 5KΩ).
- Install custom Voltage-Controlled-Crystal-Oscillator (VCXO) at U5. Please contact SIGMET for assistance in specifying this device.

For a Rev.D board the instructions are similar except that you do not need to remove any components, and should place a jumper on JP3/BC

⚠ **Warning: As noted in the previous section, for Rev.C boards U14 *Must Be Removed* whenever the VCXO phase lock mode is not being used, i.e., when the normal free-running crystal is installed.**

2.1.7 Coax Uplink and Fiber Downlink

There are two cable links between the IFD module and the RVP7/Main circuit board:

- Copper coax cable uplink from the RVP7/Main board. Provides timing information for the burst pulse window, and 16-bit data for setting the AFC output level.
- Optical fiber downlink to the RVP7/Main board. The receiver and burst pulse data samples are encoded into a 540MHz serial stream.

The uplink input from the RVP7 is an SMA input from a 75Ω shielded cable. This cable is electrically isolated from the receiver's ground (40KΩ isolation) so that noise picked up by the cable will not be coupled into the receiver circuitry. The downlink uses a 62.5/125 micron multimode optical cable terminated in type ST connectors. The coax and fiber cables can be any length up to 100 meters apiece. The RVP7 measures the round trip cable delays each time it boots up, and then uses that information to correct for range and timing offsets due to cable length.

2.1.8 Adjustments and Indicators

The IFD is packaged in a tight metal enclosure for maximum noise immunity. The only adjustments on the module are the internal gain and offset pots that adjust the AFC analog output. Two switches on the unit provide standalone test features to verify the proper functioning of the IFD and to assist with setting the voltage span of the AFC DAC.

Table 2–2: IFD Toggle Switch Settings

SW1	SW2	Function
A	A	AFC Test Low Voltage
A	B	AFC Test Midpoint Voltage
A	C	AFC Test High Voltage
B	A	Swap Burst and IF Input Signals
B	B	Normal Operation *(also labeled as "run")*
B	C	Reserved *(fiber test pattern)*
C	A	Reserved
C	B	Reserved *(fiber test pattern)*
C	C	Reserved *(fiber test pattern)*

Two LEDs provide information on the status of the module and the status of the communication to the RVP7 (fiber channel and uplink).

Table 2–3: IFD LED Indicator Interpretations

Red (Uplink)	Green (Ready)	Meaning
Blink	Blink	Reset sequence *(powerup, or from uplink)*
Blink	Off	Uplink is dead *(no signal from RVP7/Main)*
On	Off	Uplink is alive, but downlink is dead
On	On	Normal Operation *(IFD and Main are both okay)*

The internal jumper settings are summarized in the following table. Please also refer to Sections 2.1.5 and 2.1.6 for more information on setting up the AFC or External Clock options.

Table 2–4: IFD Internal Jumper Settings

	Rev.B	***Rev.C***	***Rev.D***
JP1	N/A	AB: AFC Voltage Output BC/Open: External Clock 50Ω/Open Termination	
JP2	N/A		Reserved
JP3	N/A		BC: External Clock Open: AFC Voltage Output
JP4	N/A		AB: Dither Applied to Burst Input BC: No Dither on Burst

2.1.9 Size and Mounting Considerations

The IFD is a compact sealed module with dimensions 23.6 x 10.9 x 3.0 cm. (9.3 x 4.3 x 1.2 in). The unit is designed to be mounted on edge such that the 23.6 x 3.0 cm. surface is flush on the back of the receiver cabinet with 10.9 cm. protrusion into the cabinet. The unit is typically placed where a traditional LOG receiver would be installed. The IFD is cooled by direct conduction through its metal enclosure. It should be positioned so that air can freely convect around it, or bolted to a larger surface that will conduct the heat away.

The power supply module is separate and can be mounted nearby in the radar cabinet, or it can be attached directly to the IFD using a special mounting bracket. The power supply and bracket will add 3.3 cm. (1.3 in) of overall width to the receiver module.

The power supply is a low noise, low ripple, switching unit; the input voltage range is 100–240 VAC 47–63 Hz, autoranging. The IFD has an internal 3-stage power supply input filter to minimize interference from the power cable. Nonetheless, it is still good practice to insure that the four supply wires (+5V, –12V, +12V, and Ground) be kept short and twisted together. A ferrite choke around the supply wires near the terminal strip is also recommended.

Important: The inductive filtering components inside the IFD introduce a slight voltage drop in the +5V supply. To produce the correct internal voltage, the supply voltage measured at the external terminal block should be 5.23V for Rev.D boards, and 5.17V for Rev.C and earlier boards.

Mounting space should also be reserved for the external analog anti-alias filters. These filters can be mounted in the radar cabinet itself, or they can be attached directly to the IFD on the opposite side of the power supply. The filters and mounting bracket will add 2.0 cm. (0.8 in) of overall width.

2.2 RVP7/Main Board and Chassis

The RVP7 Processor consists of a main processing board (RVP7/Main) and either one or two auxiliary processing boards (RVP7/AUX). Both boards are 9U x 280 circuit cards that insert into a standard SIGMET 3-slot enclosure. The RVP7/Main board provides the Stage 1 digital IF receiver functions and I/O functions. The Stage 2 Doppler processing functions are also computed on the RVP7/Main board, and may be expanded by using one or two RVP7/AUX boards. The Texas Instruments TMS320C40 signal processing chip is used on both boards. Note that an RVP7/Main board with a single RVP7/AUX board is approximately equivalent to an RVP6 with three RVP6/AUX boards.

The RVP7/Main inputs and outputs that are available to the user are:

- Up to 6 programmable triggers for radar control. A trigger input is also available for locking the RVP7 to an external trigger source.
- TTL transmitter pulsewidth control (4-bits).
- Optional 2-bit RS422 polarization control for ZDR measurements.
- Optional 8-bit RS422 transmit phase control for Klystron systems.
- Serial line data output and control for real time display applications.
- Serial port for local setup TTY.
- 32-bit parallel TTL AZ and EL angle inputs. These angles may also be received as a serial data stream.
- SCSI-2 interface to host computer such as a UNIX workstation running the SIGMET IRIS system. The SCSI interface transfers data to the host computer and serves to configure the RVP7. A parallel interface is also available.
- Analog I, Q and LOG output signals from 2 MHz DAC for scope monitoring with nominal 2V p-p span. These are for convenient scope monitoring.

2.2.1 Power-Up Details

Ideally, the RVP7/Main board should be powered-up after or at the same time as the IFD. This allows the diagnostic tests on the main board to run properly and exercise both components of the system. If the main board is switched on first, then all of the IFD diagnostics will fail and the RVP7 will be generally unusable, even if power were subsequently applied to the IFD.

Often the power sequencing order can not be controlled in detail, e.g., the IFD may be located in a different cabinet or a different room from the main chassis. To help in these cases, the RVP7 performs a special power sequencing reboot whenever the IFD is turned on after the Main board has already powered up. This special reboot will occur whenever a) the fiber signal was not present at boot time, b) the last boot was not a power sequencing reboot, and c) the fiber signal is detected for five continuous seconds. Thus, you may powerup your equipment in any order.

Normally the RVP7/Main board boots code from an on-board ROM (U62). However, the board is also capable of rebooting from a ROM image that is supplied by the host computer via the "BOOT" command (See Section 6.24). This makes it possible to install and run new versions of code without having to replace the boot ROM itself. Unattended remote sites can be upgraded in this manner via a network.

When the RVP7 is first powered up, it will always boot from the on-board ROM (nothing else would be possible). but the ROM is also considered the most trusted source of code, and therefore will also be used for all "hard" resets:

- External hardware $\overline{\text{RESET}}$ line (parallel interface reset)
- SCSI Bus reset sequence
- RVP7 "RESET" command with "Pwr" option selected

When the BOOT command has been used to install a new version of code, that new code will persist across all of the following types of "soft" resets:

- Autoreset performed by the internal Watchdog
- Any type of reset invoked using the "*" local TTY command
- The power sequencing reboot that occurs when the IFD is turned on after the RVP7/Main board has already powered up.
- RVP7 "RESET" command with "Rst" or "Dig" options selected

A 32-bit CRC check is included in the RVP7's boot ROM. This allows the entire ROM image to be checked for internal consistency during the startup diagnostics, and during a reboot from the host computer. An error bit is allocated in GPARM Output Word #12 to indicate a checksum failure.

The CRC check is designed to accept ROMs that are programmed from either a 0x00 or 0xFF blank state. If you are making your own ROMs from Intel Hex data files, you may use either 0x00 or 0xFF as the default value for ROM locations that are not explicitly defined by the file.

Note: SIGMET has support for third party RVP7 software developers who would like to incorporate the BOOT command into their RVP7 driver.

2.2.2 Booting Code Upgrades From IRIS

The RVP7 is able to boot from a ROM image that is supplied by the host computer. IRIS versions 7.16 and higher support automatic upgrading of RVP7 code whenever an application is started that uses the signal processor. New DSP code is loaded as needed from the IRIS_CONFIG file "dsp.rom", which typically will be a symbolic link to a particular named RVP7 ROM distribution file. No upgrade is done, and no errors are generated, if "dsp.rom" does not exist, or if it exists but has already been loaded into the RVP7.

To install new RVP7 code under IRIS, first fetch the distribution file from our FTP site and put it in your IRIS configuration directory. You must use the Intel-HEX file that has the ".hex" suffix; not the binary file that has the ".bin" suffix. Your dialog may look something like this:

```
$ cd $IRIS_CONFIG
$ ftp ftp.sigmet.com
Name: anonymous
Password: <Use your email address>
cd outgoing/releases/rvp7
binary
get rvp7-v21-u62.hex.Z
quit
```

Of course, you would substitute the most recent "–v*nn*–" version number in the file name. You then uncompress the file (it becomes plain ASCII), set its permissions to make sure it is readable, and setup a symbolic link named "dsp.rom" that points to it.

```
$ uncompress rvp7-v21-u62.hex.Z
$ chmod 644 rvp7-v21-u62.hex
$ rm -f dsp.rom
$ ln -s rvp7-v21-u62.hex dsp.rom
```

Alternatively, you can avoid most of these steps if you are running an IRIS that was recently installed from CDROM. Simply use the RVP7 code that is shipped with each IRIS release in the "config_template/init" directory:

```
$ cd $IRIS_CONFIG
$ ln -s ../config_template/init/rvp7-v21-u62.hex dsp.rom
```

Once the symbolic link is setup, whenever any IRIS process or IRIS utility wishes to open the RVP7 it will first check whether "dsp.rom" exists and points to valid data. If it does, and if the code version of the file does not match the version that is currently running, then that new code will be loaded into the RVP7. A diagnostic message will pop up from any utility that performs an automatic upgrade, and these events are also logged by IRIS/INGEST. You can manually check which version of code is running using the **dspx** utility. Use the **gparm** command within **dspx –nochat**, or the RVP7's **V** command while chatting directly with the processor.

The entire reload process takes about three seconds, but it only needs to be done once after each RVP7 cold start. The new code then continues to run in the RVP7 for as long as the processor remains powered up.

2.2.3 Radar Digital Signals

The RVP7 radar digital signals are intended to connect to a radar control unit that must be supplied by the user. Not all of the interface signals may be needed in every installation; the design approach has been to provide a wide range of control signals so that the best match for each radar can be chosen.

Users may supply the RVP7 with their own pretrigger for installations in which adequate trigger control already exists. However, a helpful alternative is to use the built-in trigger generator which supplies six independently-timed trigger waveforms at rates between 50Hz and 6000Hz with better than 0.02% accuracy. For dual-PRF velocity unfolding applications, the built-in trigger must be used. The six trigger waveforms are still output when the RVP7 is driven by an external pretrigger. The synchronization jitter between the user pretrigger and the six trigger outputs is less than 0.014 microseconds.

The RVP7's response to a missing external trigger is that the processor will insert fake (software) "triggers" at a rate of 250Hz whenever the trigger input is missing for more than 0.100 seconds. These fake triggers will keep the RVP7's internal code and external outputs running in spite of

the missing input (the data values will all be zero, and the "no trigger" bit will be set in GPARM immediate status word #1). Normal operation automatically resumes as soon as the external trigger is restored.

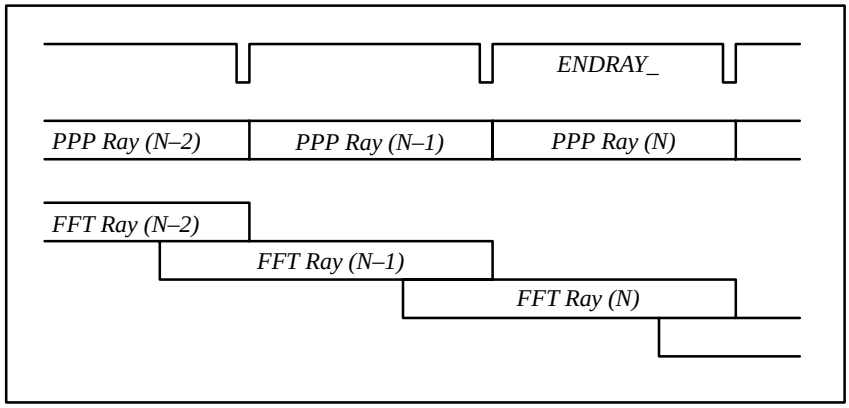
All digital outputs from the RVP7, with the exception of the three special coax cable buffers, are driven by TTL gates of either the LS or ALS variety, and standard TTL wiring practices should be used for their interconnection. Most RVP7 inputs comply with TTL voltage thresholds (0.8V max low, 2.0V min high), although the trigger input uses CMOS levels (1.5V max low, 2.5V min high) for improved noise immunity. The trigger input may also be driven as high as +100V or as low as –100V without damage. This makes it easier to connect to existing high-voltage trigger distribution systems.

Unlike the TTL outputs, the three coax drivers are designed to supply +15-Volt (open circuit) waveforms into a load impedance of 50–75Ω. These signals are intended to drive shielded cables and to connect to radar trigger or scope circuitry that may need voltages greater than the usual TTL-levels. The inputs to the drivers are brought out to the backplane so that users may jumper any signal (e.g. triggers, clocks, sampling pulses, etc.) to them for driving over long distances.

TRIGIN	CMOS-Level trigger input. One of the edges of TRIGIN is interpreted by the RVP7 as the pretrigger point; the actual pulsewidth of the signal does not matter. The delay to range zero is configured via the setup TTY.
TGEN 0–6	Trigger generator outputs. The waveforms appearing on these lines are programmed by the user to meet the radar's exact timing needs. All lines may be setup and used independently and can contain, for example, pre-trigger pulses, calibration gates, range strobes, scope triggers, etc. The first three triggers (TGEN0, TGEN1, and TGEN2) are either TTL or 0–15V levels (jumper selectable). If necessary, the second three triggers may be wired through the built-in 75Ω drivers so that all six triggers use the 0–15V levels.
A/B/C 75 IN/OUT	Three uncommitted 75Ω coaxial cable drivers for digital output of zero to +15V. The IN lines may be tied to any backplane signal that must be sent over a long coax wire.
ENDRAY_	TTL-Level active-low output pulse of 1.0 µsec duration, which indicates that the RVP7 has just finished, acquiring the last pulse that will contribute to a given ray of data. The interpretation of this signal is slightly different for the Pulse-Pair modes compared with the "batched" modes (FFT, Random Phase, DPRT, etc.). Figure 2–3 shows the timing of ENDRAY_ relative to the received pulses that contribute to each ray. The Pulse-Pair rays are non-overlapping; hence ENDRAY_ not only marks the end of one ray, but also the beginning of the next. The batched rays, on the other hand, are allowed to overlap. Although ENDRAY_ continues to mark the final pulse of each batched ray, those times do not necessarily coincide with the first pulse used by the next ray. The ENDRAY_ signal is intended to synchronize external hardware to the RVP7's ray processing boundaries. Unless you actually have

additional equipment of this sort, the ENDRAY_ signal can usually be ignored.

Figure 2–3: Timing of pulses that contribute to each ray, relative to ENDRAY_



SCLK_

This TTL output line is low during the intervals of time that "I" data are being computed by the FIR filter chips. Thus, it serves as an approximate indicator of the location of the RVP7's range bins. Because the FIR calculations are heavily pipelined, the phase of this signal will be shifted slightly from the exact bin intervals. However, the frequency will be precisely representative of the bin spacing.

PHOUT0–7 +/–

These are eight RS422 differential drivers that can be used to control the phase of a coherent radar transmitter. These signals share some of the same I/O pins that are used by the parallel interface, and thus, are only available when the SCSI interface is used. For systems that do not need all eight phase control lines, PHOUT6 and PHOUT7 can be reassigned (with jumpers) to differentially drive the two polarization lines POLAR0 and POLAR1. Note that either "+" or "–" signals can be used individually if single-ended TTL output levels are preferred.

The eight control lines can also be redefined (via setup) to serve as Digital AFC control outputs.

POLAR 0/1

TTL-Level or RS422 polarization control output lines. These signals remain at a steady level during either fixed horizontal or vertical processing, and alternate from pulse to pulse during ZDR processing. The timing and sense of the signals is set in software. The RS422 levels are obtained by jumpering the drivers that usually supply PHOUT6/7 (See JP23/24 description in Section 2.2.7).

PWBW 0–3

These four lines may be programmed to assume whatever bit patterns are required to set the pulsewidth of the transmitter. Up to four different pulsewidths are supported.

TAG 0–31

Thirty two TTL-Level input lines. These are sampled by the RVP7, and the bits accompany each processed output ray (See PROC command, Section 6.7). The inputs can also be read directly via the

GPARM command (See Section 6.9). The interpretation of theses lines is largely decided by the user, but typically antenna azimuth is wired to TAG 0–15 and antenna elevation is wired to TAG 16–31. The RVP7 supports an antenna synchronizing mode that assumes this wiring arrangement. Whenever TAG data are required, the processor reads TAG 0–15 up to ten times in a row (spaced by 0.5 μsec) until two successive values compare equal. This is done so that unsynchronized input data will be latched in a valid state. If after ten retries the lines were never observed in a consistent state, then the last observed state is used. Likewise, TAG 16–31 are repetitively sampled as a group.

2.2.4 Backpanel Digital AFC Outputs

The RVP7/Main board supports digital AFC output from the chassis backpanel, in addition to the traditional analog AFC that is driven by a voltage level from the IFD. The availability of these digital outputs makes the RVP7 compatible with newer STALOs that use digital frequency synthesis (rather than a VCO) as their method of tuning.

The RVP7's eight RS422 "phase control" outputs can be redefined to function as AFC control lines. This represents an efficient use of these hardware lines, i.e., a magnetron (non synchronous) radar usually needs frequency control but can not modulate phase; whereas a klystron (or other synchronous) radar may need to modulate phase but does not need to control frequency. Thus, the two functions tend to be mutually exclusive.

The digital AFC control cable must run between the STALO and the RVP7/Main chassis, not the IFD box. This is likely to be a longer cable run, but the RS422 signals are specified for distances up to 100 meters. Still, cable noise and ground loops may be a problem with long cable runs, and an alternate wiring approach is to interface to the coax uplink itself (Section 2.5.1), perhaps by using the DAFC Module (Section 2.4).

As an example, suppose that we have a digital STALO with BCD input in 100kHz steps, an upper sideband 30MHz IF, and a magnetron that needs to be tracked in the range 5605–5609 MHz. Our STALO must therefore cover the range 5635–5639MHz. This can be done by selecting BCD format, and wiring the two 4–bit decimal digits to the units and tenths MHz STALO inputs. Configure [–100%,+100%] to map into [50,90], and wire the remaining STALO inputs to "563x.x" Finally, set the AFC hysteresis limits to something like 55KHz/70KHz. During tracking, the AFC loop will request a correction whenever the frequency error is greater than 70KHz. But since the nearest 100kHz click will always be within 50KHz of center, the inner limit will eventually be reached and the loop will lock.

Additional information about using AFC can be found in Sections 2.1.5, 2.4, 3.3.6, and 5.1.2.

2.2.5 SCSI Interface Signals

The Small Computer System Interface (SCSI) is a standard interface on many workstations and personal computers, and is supported on RVP7. There are several variants on the SCSI specification, not all of which are electrically or mechanically compatible with each other. The

RVP7 supports the single ended SCSI-I protocol, but can also be used in almost all single ended SCSI-II systems. Either the mini 50-pin connector, or the Centronics 50-pin connector may be used, though the RVP7 back panel supports only the later. The electrical and timing specifications for SCSI, as well as the command and message description formats, are available as ANSI publication X3.131.

To configure the RVP7 as a SCSI device you must set jumpers JP17 and JP18 to the "BC" position. If on-board termination is used, then 220/330Ω resistor packs should be installed at U103 and U104, otherwise these sockets should be empty. In the on-board case, to use terminator power from the SCSI bus itself set JP19 to "AB"; the "BC" position powers U103 and U104 from the internal +5V supply. Lastly, set the SCSI address using JP20, 21 and 22.

The RVP7 responds to the the following subset of the SCSI programming standard:

Target Select Sequence & IDENTIFY Message

The RVP7 responds as a target device on the SCSI bus. When an initiator device addresses the RVP7, the RVP7 cycles through the SCSI bus selection phases, and interprets the accompanying IDENTIFY message from the initiator. This message contains the target LUN (which is ignored), and a bit which indicates whether the RVP7 is permitted to disconnect from the bus.

The RVP7 terminates all successful SCSI commands by sending the COMMAND COMPLETE message. This message is also sent for the (hundreds of) SCSI commands that are ignored by the RVP7. The MESSAGE REJECT message is sent whenever the RVP7 receives a message that is not implemented.

Bus Disconnection and ReSelection

The RVP7 always releases the SCSI bus upon completion of each SCSI command. However, the RVP7 can also release the bus in the middle of a SEND or RECEIVE command, if the data transfer must be delayed for any reason. This can happen when the initiator tries to read more words than are presently available in the RVP7 output FIFO. It can also happen when the initiator writes data faster than the RVP7 can accept it. When, at some later time, the data transfer can again proceed, the RVP7 reselects the initiator and continues where it left off. To accomplish these transactions, the RVP7 uses the following messages to the initiator:

- SAVE DATA POINTER
- RESTORE POINTERS
- DISCONNECT
- IDENTIFY

SYNCHRONOUS DATA TRANSFER REQUEST Message

This message is used to arbitrate the type of data transfer that the initiator and target devices use. The RVP7 only supports the asynchronous transfer mode, and thus always responds with the message:

```
0x01  0x03  0x01  0x00  0x00
```

INQUIRY Command

The RVP7 functions as a processor type device on the SCSI bus, and responds to a SCSI INQUIRY command with the following 36-byte sequence:

```
 Byte    0      3       (Indicates processor device)
 Byte    1      0
 Byte    2      1       (Indicates ANSI Approved Version)
 Byte    3      0
 Byte    4     31       (Additional length in bytes)
Bytes  5– 7     0
Bytes  8–15    "SIGMET  "
Bytes 16–31    "RVP7            "  or  "RVP6–2          "
               (Depending on RVP6 emulation option)
Bytes 32–35    "Vnn "  (nn is code rev. level in decimal)
```

MODESENSE Command

This command returns a 10-byte sequence in which the first two bytes indicate the number of 16-bit words that are available to be read from the RVP7. This value is often useful in deciding how many words to read in the next RECEIVE command.

```
 Byte  0       Low 8-bits of output count
 Byte  1       High 8-bits of output count
Bytes 2-9      Unused (Zero)
```

SEND and RECEIVE Commands

All I/O for the RVP7 command set described in Chapter 6 takes place using the SCSI SEND and RECEIVE commands. You must organize the 16-bit command and data words into an 8-bit stream that can be sent on the SCSI bus. A TTY setup question in the RVP7 permits swapping the bytes in the 16-bit words to match the integer*2 format of the host computer.

2.2.6 Parallel Interface Signals

The parallel TTL interface is no longer supported. Legacy hardware should continue to work.

2.2.7 Jumper Settings

The RVP7/Main processor board has several jumpers that are used for configuration. All of these jumpers consist of a three pin header with pins labeled "A," "B," and "C." A jumper is installed either to connect pins A-B, or pins B-C. Thus all of the jumpers are always plugged in somewhere on the board.

Note: The silkscreen printing on some revisions of the circuit board may identify the jumper's "A" pin with a triangular symbol, rather than with the letter "A". The "B" and "C" pins are implied but not labeled in that case.

Note: The 14-pin header at the top edge of the board is a JTAG diagnostic connector which should never have any jumpers plugged onto it.

Note: Factory defaults are indicated by **bold** print.

JP1 **AB = Use internal clock on serial interface transmission**
BC = Use external clock on serial interface transmission

```
JP2   AB = Use internal clock on serial interface reception
      BC = Use external clock on serial interface reception

JP3   AB = High-Byte-First (HP,IBM,SGI) I/O byte ordering
      BC = Low-Byte-First (PC,DEC) I/O byte ordering

      (Note: JP3 is set at the factory per the expected customer application.)

JP4   AB = Setup terminal runs at 9600 baud
      BC = Setup terminal runs at configured baud rate

JP5   AB = Nonvolatile RAM writing is disabled
      BC = Nonvolatile RAM is enabled

JP6   AB = External JTAG clock     \ For Rev.A
      BC = Internal JTAG clock     /   boards

      AB = All DSPs in JTAG loop   \ For  Rev. B
      BC = Master DSP in JTAG loop /  & higher

JP7   AB = User RESET_ line (P1,A20) has no effect
      BC = User RESET_ line (P1,A20) enabled

JP8   AB = TGEN0 is 0–15V signal
      BC = TGEN0 is TTL signal

JP9   AB = TGEN1 is 0–15V signal
      BC = TGEN1 is TTL signal

JP10  AB = TGEN2 is 0–15V signal
      BC = TGEN2 is TTL signal

JP11  AB = Terminate external trigger into 75Ω
      BC = Do not terminate external trigger

JP12  AB = PULLD Signal on P1,C30 held low
      BC = PULLD Signal on P1,C30 held high

JP13  AB = PULLC Signal on P1,C29 held low
      BC = PULLC Signal on P1,C29 held high

JP14  AB = PULLB Signal on P1,C28 held low
      BC = PULLB Signal on P1,C28 held high

JP15  AB = PULLA Signal on P1,C27 held low
      BC = PULLA Signal on P1,C27 held high

JP16  AB = External I/O terminator power
      BC = Internal +5V terminator power (Must use for parallel I/O)
```

Jumpers JP17 and JP18 select the I/O protocol that will be used for communication with the host computer.

JP17	JP18	
AB	AB	DEC DR11 Parallel
AB	BC	Hewlett Packard GPIO Parallel
BC	AB	*-reserved-*
BC	**BC**	**SCSI**

Jumpers JP19/20/21/22 select auxiliary settings for the I/O protocol that is set by JP17/18. In the parallel modes the four jumpers determine the polarity of the handshake control lines. In SCSI mode three of the jumpers determine the SCSI bus address, and the fourth (JP19) is unused.

```
JP19  AB = IOACK Active Low
      BC = IOACK Active High

JP20  AB = IOAUX Active Low
      BC = IOAUX Active High

JP21  AB = IOREQ Active Low
      BC = IOREQ Active High

JP22  AB = WRITE Active Low
      BC = WRITE Active High
```

JP20	JP21	JP22		
BC	BC	BC	SCSI ID 0	
BC	BC	AB	SCSI ID 1	
BC	AB	BC	SCSI ID 2	
BC	AB	AB	SCSI ID 3	
AB	**BC**	**BC**	**SCSI ID 4**	**Default SCSI ID used by SIGMET**
AB	BC	AB	SCSI ID 5	
AB	AB	BC	SCSI ID 6	
AB	AB	AB	SCSI ID 7	

Note: The continuous test mode is entered on powerup if jumpers JP17–JP22 are set to the (somewhat illegal) pattern: JP17:BC, JP18:BC, JP19:AB, JP20:AB, JP21:AB, JP22:AB. See Section 3.1.3 for more details.

The following jumpers are available on Rev. B (and greater) boards. They determine whether the RS422 signals PHOUT6+/PHOUT6– and PHOUT7+/PHOUT7– serve as phase control or polarization control lines.

```
JP23  AB = RS422 drivers for PHASE6
      BC = RS422 drivers for POLAR0

JP24  AB = RS422 drivers for PHASE7
      BC = RS422 drivers for POLAR1
```

2.2.8 RVP7/Main Board Pin Assignments

A serial RS232/RS423 TTY may be plugged into the RVP7 to carry out the local setup functions. A standard 6-pin MMJ connector is provided for a quick and simple hookup. The TTY signals are also available on the DIN edge connectors if a permanent wiring arrangement is preferred.

Table 2–5: MMJ Connector P7 Pin Assignments

Pin	Signal Name	RVP7 Connection
1	DTR	Logic High
2	Transmit data+	RS432 data out
3	Transmit data–	Ground
4	Receive data–	RS432 input data–
5	Receive data+	RS432 input data+
6	DSR	No connection

The pin assignments for the three 96-pin DIN edge connectors are given in Table 2–6. Each connector consists of three rows of 32 pins. The connectors are labeled "1," "2," and "3;" the rows are labeled "A," "B," and "C." Power connections are indicated by "GROUND," "+5V," "–15V," and "+15V." In addition, pins labeled "Rsrv" are reserved for additional power connections and should not be used for signal connections. Note that "GND" indicates signal ground, which is different from supply ground. GROUND pins are used to supply operating current to the circuit board and act as returns for all power supplies. GND pins are ground reference points for input and output signals and, in general, carry very little current.

Table 2–6: SCSI Interface, DIN Connector Pin Assignments

Pin	A1	B1	C1	A2	B2	C2	A3	B3	C3
1	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND
2	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V
3	–DB0	GND	PHOUT0+	LED3C	---	LED3A	TAG0	IBBOOT_	TAG16
4	–DB1	GND	PHOUT0–	SPARE0	SPARE6	SPARE7	TAG1	IBDCLR_	TAG17
5	–DB2	GND	PHOUT1+	SPARE1	IVID+	IVID–	TAG2	IBDCLK	TAG18
6	–DB3	GND	PHOUT1–	SPARE2	SPARE8	SPARE9	TAG3	IBSEL3	TAG19
7	–DB4	GND	PHOUT2+	SPARE3	QVID+	QVID–	TAG4	IBSEL4	TAG20
8	–DB5	GND	PHOUT2–	SPARE4	SPARE10	SPARE11	TAG5	IBSEL5	TAG21
9	–DB6	GND	PHOUT3+	SPARE5	LVID+	LVID–	TAG6	IBSEL6	TAG22
10	–DB7	GND	PHOUT3–	---	---	---	TAG7	IBSEL7	TAG23
11	–DBP	GND	PHOUT4+	TIOXMT	---	---	TAG8	IBSEL8	TAG24
12	–ATN	GND	PHOUT4–	TIORCV	TIOGND	---	TAG9	IBSEL9	TAG25
13	–BSY	GND	PHOUT5+	POLAR0	GND	TRIGIN	TAG10	IBSEL10	TAG26
14	–ACK	GND	PHOUT5–	POLAR1	GND	UPLINK	TAG11	IBSEL11	TAG27
15	–RST	GND	PHOUT6+	PWBW0	GND	---	TAG12	IBSEL12	TAG28
16	–MSG	GND	PHOUT6–	PWBW1	GND	---	TAG13	IBSEL13	TAG29
17	–SEL	GND	PHOUT7+	PWBW2	GND	SCLK_	TAG14	IBSEL14	TAG30
18	---	GND	PHOUT7–	PWBW3	GND	ENDRAY_	TAG15	IBSEL15	TAG31
19	---	GND	---	TGEN0	GND	TGEN3	IBD0	IBSEL16	IBD9
20	---	GND	---	TGEN1	GND	TGEN4	IBD1	IBSEL17	IBD10
21	---	GND	---	TGEN2	GND	TGEN5	IBD2	IBSEL18	IBD11
22	–C/D	GND	---	A75IN	GND	A75OUT	IBD3	IBSEL19	IBD12
23	GND	GND	GND	B75IN	IBDNRDY_	B75OUT	IBD4	IBSEL20	IBD13
24	–REQ	GND	---	C75IN	IBDNSTB_	C75OUT	IBD5	IBSEL21	IBD14
25	–I/O	GND	GND	LED1C	IBDND2	LED1A	IBD6	IBSEL22	IBD15
26	---	---	---	LED2C	IBDND3	LED2A	IBD7	---	IBD16
27	SIORCLK	SIORCV	---	IBDND0	IBDND4	IBDND6	IBD8	IBUPRDY_	IBD17
28	SIOXCLK	SIOXMT	---	IBDND1	IBDND5	IBDND7	IBUPD0	IBUPSTB_	IBUPD5
29	SIOICLK	SIORTS	---	–15V	–15V	–15V	IBUPD1	IBUPD3	IBUPD6
30	SIOGND	SIOCTS	---	+15V	+15V	+15V	IBUPD2	IBUPD4	IBUPD7
31	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V
32	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND

2.3 RVP7 Auxiliary Processing Board (RVP7/AUX)

The RVP7/AUX Auxiliary Processing Board is designed as a plug-on addition to the basic single-board RVP7/Main signal processor. Each RVP7/AUX board adds ten TMS320C40 DSP chips (the main board has 4), and an additional 5.0 MegaBytes of storage (the main board has 2.5MB). The auxiliary boards operate as slave processors to the RVP7/Main board. Identical copies of the processing code are downloaded from the main board, and the digitized "I" and "Q" data stream is shared among all boards via an 18-bit parallel bus. Communication between boards is via a 7-MegaByte/second serial stream. Either one or two auxiliary boards may be connected in a single system.

When the RVP7/Main first powers up, it queries its expansion bus to determine whether any RVP7/AUX boards are connected. It automatically uses as many boards as it can find; there are no jumper or configuration changes that need to be made. When RVP7/AUX boards are added, the overall processing speed increases by approximately x4.3 (one additional board) and x7.7 (two additional boards).

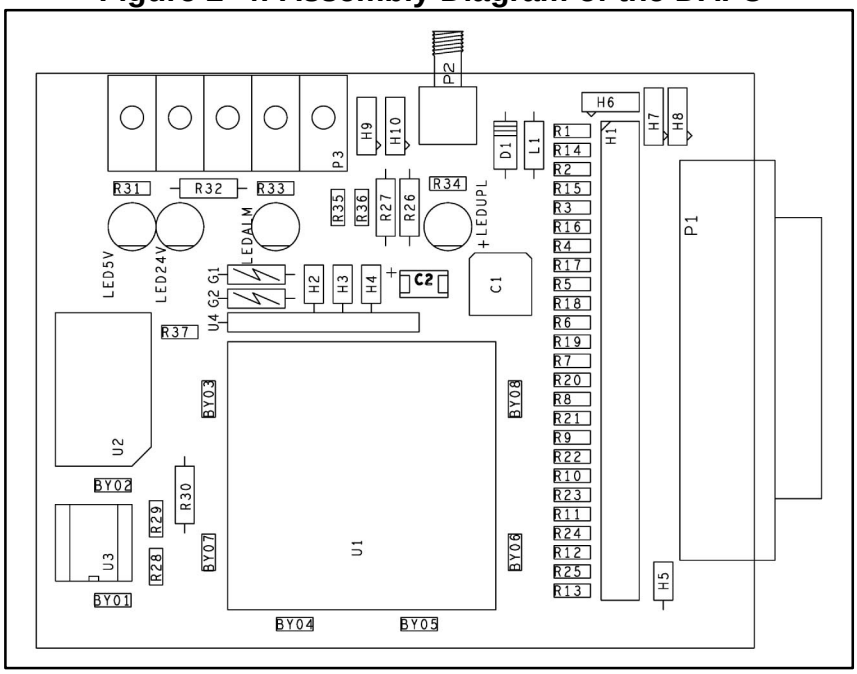
Table 2–7: RVP7/AUX Board DIN Connector Pin Assignments

Pin	A1	B1	C1	A2	B2	C2	A3	B3	C3
1	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND
2	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V
3	---	---	---	---	---	---	---	IBBOOT_	---
4	---	---	---	SPARE0	---	---	UPUPRDY_	IBDCLR_	DNUPRDY_
5	---	---	---	SPARE1	---	---	UPUPSTB_	IBDCLK	DNUPSTB_
6	---	---	---	SPARE2	---	---	UPUPD0	IBSEL0	DNUPD0
7	---	---	---	SPARE3	---	---	UPUPD1	IBSEL1	DNUPD1
8	---	---	---	SPARE4	---	---	UPUPD2	IBSEL2	DNUPD2
9	---	---	---	SPARE5	---	---	UPUPD3	IBSEL3	DNUPD3
10	---	---	---	SPARE6	---	---	UPUPD4	IBSEL4	DNUPD4
11	---	---	---	SPARE7	---	---	UPUPD5	IBSEL5	DNUPD5
12	---	---	---	SPARE8	---	---	UPUPD6	IBSEL6	DNUPD6
13	---	---	---	SPARE9	---	---	UPUPD7	IBSEL7	DNUPD7
14	---	---	---	SPARE10	---	---	---	IBSEL8	---
15	---	---	---	SPARE11	---	---	UPDNRDY_	IBSEL9	DNDNRDY_
16	---	---	---	---	---	---	UPDNSTB_	---	DNDNSTB_
17	---	---	---	---	---	---	UPDND0	---	DNDND0
18	---	---	---	---	---	---	UPDND1	---	DNDND1
19	---	---	---	---	---	---	UPDND2	---	DNDND2
20	---	---	---	---	---	---	UPDND3	IBD4	DNDND3
21	---	---	---	---	---	---	UPDND4	IBD5	DNDND4
22	---	---	---	---	---	---	UPDND5	IBD6	DNDND5
23	---	---	---	---	---	---	UPDND6	IBD7	DNDND6
24	---	---	---	---	---	---	UPDND7	IBD8	DNDND7
25	---	---	---	---	---	---	---	IBD9	---
26	---	---	---	---	---	---	IBD0	IBD10	IBD14
27	---	---	---	---	---	---	IBD1	IBD11	IBD15
28	---	---	---	---	---	---	IBD2	IBD12	IBD16
29	---	---	---	---	---	---	IBD3	IBD13	IBD17
30	---	---	---	---	---	---	---	---	---
31	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V
32	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND

2.4 Digital AFC Module (DAFC)

The DAFC is a small self-contained circuit board which can passively "eavesdrop" on the RVP7's serial uplink transmissions. Its purpose is to generate a set of digital AFC control lines that could be applied, for example, to a custom STALO frequency synthesizer. A full size (3"x3.75") assembly diagram of the board is shown in Figure 2–4. It can be installed in the radar system either as a bare board, or packaged into a small metal enclosure.

Figure 2–4: Assembly Diagram of the DAFC



SIGMET recommends that the DAFC board be used in new system designs whenever AFC is required, as it offers these advantages over other methods of frequency control:

1) The use of a digital frequency synthesizer is superior to using analog AFC because the stability of a synthesized STALO can be made much greater than that of a tunable cavity oscillator. Also, noise on the AFC control voltage directly contributes to phase noise in the received weather targets in analog AFC systems, so cabling of the control signal can become tricky.

2) Using the DAFC board is preferable to using the 8-bit AFC backpanel option of the RVP7/Main chassis, because the board can be physically located very close to the STALO. The length of the control cable and its susceptibility to noise and ground loops are therefore reduced. Also, the DAFC board can supply up to 24 output control lines, rather than just eight.

The digital output lines are made available as TTL levels on a 25-pin female "D" connector (P1). There are 130Ω resistors (R1–R25) in series with each output line to help protect the board against momentary application of non-TTL voltages on its external pins. However, these resistors do impose a restriction on the input line configuration of the receiving device. To assure a valid TTL low level of 0.6V max. requires that the STALO inputs be pulled up to +5

with nothing less than (approx.) 1.2KΩ. Put another way, the low level input current of the receiving device should not exceed 4.5mA. Most STALOs that we have seen use 5-20KΩ pull-up resistors, so this should not be a problem.

All twenty five pins of the "D" connector are wired identically on the DAFC board, i.e., each pin connects to one end of a 2-pin jumper (2x25 header H1), the other end of which connects to a Programmable Logic Device (PLD) chip. The PLD lines can be configured either as inputs or outputs, and this single chip handles all of the decoding and driving needs for the entire board. For each "D" connector pin that is to be used as an AFC output or Fault Status input, you should install the corresponding jumper to connect that pin through to the PLD, or use a wirewrap wire if the pin must go to a different PLD line. The "D" connector pin numbers are printed next to each of the jumper locations. Because of the ordering of the pins in the connector housing, jumpers 1 through 13 are interleaved with jumpers 14 through 25.

The uplink protocol that the board should be expecting is selected by jumpers H3 and H4, as summarized in Table 2–8. The first three table entries describe three fixed mappings of the traditional AFC-16 uplink format onto various pins of the 25-pin "D" connector. One of these choices must be used whenever the DAFC is interfaced to an RVP7 system whose uplink uses the older style 16-bit AFC uplink format. In this case you will have to make most or all of the pin assignments using wirewrap wire to connect each bit to its corresponding pin. This will be somewhat tedious, but hopefully one of the three formats will be a reasonable starting point for doing the wiring. By far the most preferable solution, however, is to use the Pinmap uplink protocol (available since Rev.19) which allows for complete software mapping of all 25 external pins.

Table 2–8: DAFC Protocol Jumper Selections

H4	H3	Function
On	On	AFC-16 format, Bits<0:15> on Pins<1:16>, Fault input on Pin 25
On	Off	AFC-16 format, Bits<0:15> on Pins<25:10>, Fault input on Pin 3
Off	On	AFC-16 format, Bits<0:15> on Pins<18, 19, 6, 7, 21, 22, 23, 11, 10, 9, 20, 8, 12, 25, 13, 24>, Fault input on Pin 4
Off	Off	Pinmap format, software assignment of all pins

Ground, +5V, and +24V power supply pins on the "D" connector should be connected with wirewrap wire to the nearby power and ground posts H6, H7, and H8. The PLD jumpers for these power supply pins must not be installed. Two 3K/6K resistive terminators are also available at H5 for pulling pins up to approximately +3.3V when that is appropriate. Unused "D" connector pins should remain both unwired and not jumpered.

⚠ **Warning: It is important that the jumpers only be installed for pins that carry TTL inputs or outputs destined for the on-board PLD. The jumpers must be removed for all power supply pins, and for unused and reserved pins of the external device.**

The DAFC board runs off of a single +5V power supply which can be applied either from the STALO through the "D" connector, or externally through the terminal block. There are also provisions for supplying +24V (approx.) between the terminal block and the "D" connector, which is handy for cabling power to a STALO that requires the second voltage. Two green LEDs indicate the presence of +5V and +24V. Terminal block Pin #1 is +5V, Pin #2 is +24V, and Pin#3 is Ground. Pin #1 is the one nearest the corner of the board.

There is an option for having a "Fault Status" input on the "D" connector of the DAFC. Since the board is completely passive in its connection to the uplink, the fault status bit will not affect the uplink in any way. Rather, the bit is simply received by the board (with optional polarity reversal) and driven onto the terminal block (P3) from whence it can be wired to some other device, e.g., a BITE input line of an RCP02. A yellow LED is included to indicate the presence of any external fault conditions.

The "AB" position of the 3-pin "Alarm" jumper (H9) connects the Fault Status signal to Pin #4 of the terminal block, whereas the "BC" position grounds that terminal block pin. A second ground can be made available at Pin #5 of the terminal block by installing a jumper in the "BC" position of the "Spare" 3-pin jumper (H10). This second ground could be used as a ground return when the Fault Status line is driven off of the terminal block. The "AB" position of the "Spare" jumper is reserved for some future input or output line on the terminal block.

Both the shield and the center conductor of the uplink SMA input connector (P2) are electrically isolated (> 100KΩ) from the rest of the DAFC board. Moreover, the SMA connector pins themselves are high-impedance and unterminated. What this means is that the board can be TEE'd into the uplink cable anywhere in the cable run from the RVP7/Main board to the IFD. Since the cable is driven by the RVP7/Main, it must be at one end of the cable; and since termination is provided by the IFD, it must be at the other end. The DAFC can be anywhere in the middle. Be sure, however, that the TEE is located right at the DAFC itself so that an unterminated cable stub is not created. A red LED is included to indicate that a valid uplink data stream is being received.

A crystal oscillator is used to supply the operating clock for the on-board logic, and there are two choices of frequency to use. If jumper H2 is "Off" then the crystal frequency should be equal to the IFD's sampling clock f_{aq}, and if H2 is "On" the frequency should be $(0.75 \times f_{aq})$.

Additional information about using AFC can be found in Sections 2.1.5, 2.2.4, 3.3.6, and 5.1.2.

2.4.1 Example Hookup to a CTI "MVSR-xxx" STALO

Here is a complete example of what would need to be done in hardware and software to interface the DAFC to a Communication Techniques Inc. digital STALO. The electrical interface for the STALO is via a 26-pin ribbon cable which carries both Control and Status, as well as DC power. This cable can be crimped onto a mass-terminated 25-pin "D" connector (with one wire removed) and plugged directly into the DAFC. The resulting pinout is shown in Table 2–9.

The STALO frequency is controlled by a 14-bit binary integer whose LSB has a weight of 100 KiloHertz. In addition, the "Inhb" pin must be low for the STALO to function. Power is supplied on the +5V and +24V pins, and two grounds are provided. An "alarm" output is also available.

Table 2–9: Pinout for the CTI "MVSR-xxx" STALO

Ribbon Pin	"D" Pin	Function	Ribbon Pin	"D" Pin	Function
1	1	Ground	2	14	--
3	2	+5V	4	15	--
5	3	+24V	6	16	--
7	4	Alarm	8	17	--
9	5	--	10	18	Bit-0
11	6	Bit-2	12	19	Bit-1
13	7	Bit-3	14	20	Bit-10
15	8	Bit-11	16	21	Bit-4
17	9	Bit-9	18	22	Bit-5
19	10	Bit-8	20	23	Bit-6
21	11	Bit-7	22	24	Ground
23	12	Bit-12	24	25	Bit-13
25	13	Inhb	26	--	--

First configure the IFD pins themselves. Pins 1 and 24 are power supply grounds, and are connected with wirewrap wire to the nearby ground posts. Pins 2 and 3 supply +5V and +24V to the STALO, and should be wirewrapped to the internal power posts. The STALO power, as well as the DAFC power, is then supplied externally via the terminal block on the DAFC itself.

Sixteen jumpers should be installed to connect the Control and Status lines, i.e., pins 4, 6–13, 18–23, and 25. We will use pinmap uplink protocol, so H3 and H4 are removed; and a x1 on-board crystal, so H2 is also removed.

The STALO has an output frequency range from 5200–6020MHz in 100KHz steps. In this example we will assume that we need an AFC frequency span of 5580–5600MHz. This can be done with the following setups from the **Mb** section:

```
AFC span– [–100%,+100%] maps into [ 3800 , 4000 ]
AFC format– 0:Bin, 1:BCD, 2:8B4D: 0,  ActLow: NO
AFC uplink protocol– 0:Off, 1:Normal, 2:PinMap : 2
  PinMap Table (Type '31' for GND, '30' for +5)
  ---------------------------------------------
  Pin01:GND  Pin02:GND  Pin03:GND  Pin04:GND  Pin05:GND
  Pin06:02   Pin07:03   Pin08:11   Pin09:09   Pin10:08
  Pin11:07   Pin12:12   Pin13:GND  Pin14:GND  Pin15:GND
  Pin16:GND  Pin17:GND  Pin18:00   Pin19:01   Pin20:10
  Pin21:04   Pin22:05   Pin23:06   Pin24:GND  Pin25:13
  FAULT status pin (0:None): 4,  ActLow: NO
```

We map the AFC interval into the numeric span 3800–4000, and choose the "Bin" (simple binary) encoding format. The actual frequency limits therefore match the desired values:

5200MHz + (3800 x 100KHz) = 5580MHz
5200MHz + (4000 x 100KHz) = 5600MHz

The "Inhb" line is held low, and fault status is input on Pin 4. Note that all pins that are not directly controlled by the software uplink (e.g., power pins, and unused pins) are merely set to "GND" in the setup table.

2.4.2 Example Hookup to a MITEQ "MFS-xxx" STALO

The electrical interface for this STALO uses a 25-pin "D" connector with the following pin assignments

- GROUND on pins 1 and 2.
- Four BCD digits of 1KHz, 10KHz, 100KHz, and 1MHz frequency steps, using Pins <25:22>, <21:18>, <17:14>, <13:10>.
- Seven binary bits of representing 10MHz steps, Bits<0:6> on Pins<9:3>.

First configure the IFD pins themselves. Pins 1 and 2 are ground, and are connected with wirewrap wire to the nearby ground posts. Pins 3 through 25 all are signal pins, so we plug in a jumper for each of these 23 pins. We will use pinmap uplink protocol, so H3 and H4 are removed; and a x1 on-board crystal, so H2 is also removed.

In this example we will assume that we wish to control the STALO in 20KHz steps from 1.350GHz to 1.365GHz. This can be done with the following setups from the **Mb** section:

```
AFC span– [–100%,+100%] maps into [ 1350000 , 1365000 ]
AFC format– 0:Bin, 1:BCD, 2:8B4D: 2,  ActLow: NO
AFC uplink protocol– 0:Off, 1:Normal, 2:PinMap : 2
  PinMap Table (Type '31' for GND, '30' for +5)
  ----------------------------------------
  Pin01:GND  Pin02:GND  Pin03:22   Pin04:21   Pin05:20
  Pin06:19   Pin07:18   Pin08:17   Pin09:16   Pin10:15
  Pin11:14   Pin12:13   Pin13:12   Pin14:11   Pin15:10
  Pin16:09   Pin17:08   Pin18:07   Pin19:06   Pin20:05
  Pin21:GND  Pin22:GND  Pin23:GND  Pin24:GND  Pin25:GND
  FAULT status pin (0:None): 0,  ActLow: NO
```

We map the AFC interval into a numeric span from 1350000 to 1365000, and choose the "8B4D" mixed-radix encoding format. The STALO itself has 1KHz frequency steps, but the AFC servo will be easier to tune if we intentionally degrade this to 20KHz. This is done simply by grounding all four of the 1KHz BCD input lines, plus the LSB of the 10KHz BCD digit. A more creative use for one of these unused pins would be to remove the pin 25 jumper, wirewrap pin 25 to ground (so the STALO sill reads it a logic low), and assign pin 25 as a fault status input. That pin could then be connected to an external fault line, if the STALO has one.

2.5 RVP7 Custom Interfaces

This section describes some additional points of interface to the RVP7. These hookups are less conventional than the "standard" interfaces described earlier in this chapter, but they sometimes can supply exactly what is needed in exactly the right place. For the most part, these custom interfaces are merely taps into existing internal signals that would not normally be seen by the user.

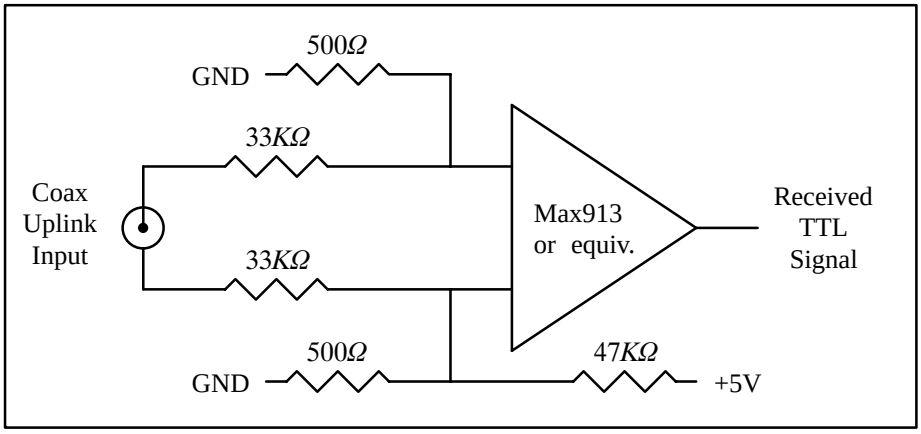
2.5.1 Using the IFD Coax Uplink

The Coax Uplink is the IFD's single line of communication from the RVP7/Main processor board. All of the information that is needed by the IFD arrives through this uplink; and as such, this signal might contain information that is also useful for other parts of the radar system. In particular, it is a convenient source of digital AFC, along with reset and other status bits, plus limited trigger timing information.

The uplink is a single digital transmission line that carries a hybrid serial protocol. The two logic states, "zero" and "one" are represented by 0-Volt and +15-Volt (open circuit) electrical levels. The output impedance of the uplink driver is approximately 55Ω. When the cable is terminated in 75Ω by an internal resistor in the IFD, the overall positive voltage swing will be approximately 8.6-Volts.

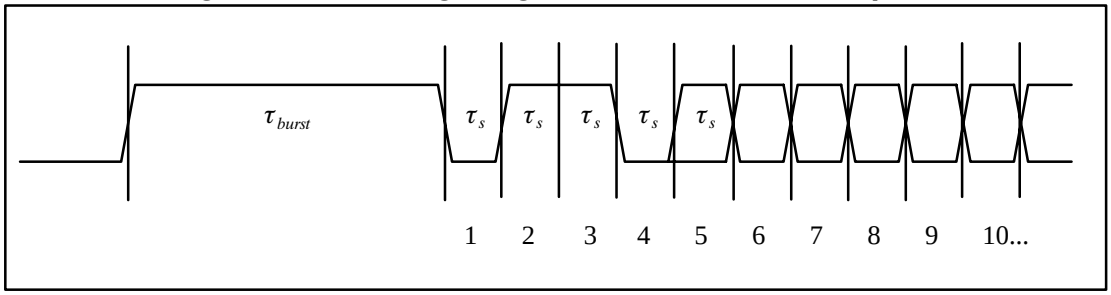
The electrical characteristics of the uplink have been optimized for balanced "groundless" reception, so that external noise and ground loop currents will not be introduced into the IFD. The recommended eavesdropping circuit is shown in Figure 2–5, and consists of a high speed comparator (Maxim MAX913, or equivalent) and input conditioning resistors. Both the shield and the center conductor of the coax uplink feed the comparator through 33KΩ isolation resistors; no direct ground attachment is made to the shield itself. The 500Ω resistors provide the local ground reference, and the 47KΩ resistor supplies a bias to shift the unipolar uplink signal into a bipolar range for the comparator.

Figure 2–5: Recommended Receiving Circuit for the Coax Uplink



The uplink signal, shown in Figure 2–6, is periodic at the radar pulse repetition frequency, and conveys two distinct types of information to the IFD. The signal is normally low most of the time (to minimize driver and termination power), but begins a transition sequence at the beginning of each transmitted pulse.

Figure 2–6: Timing Diagram of the IFD Coax Uplink



The first part of each pulse sequence is a variable length "burst window" which is centered on the transmitted pulse itself, and which has a duration τ_{burst} approximately 800ns greater than the length of the current FIR matched filter. The burst window defines the interval of time during which the IFD transmits digitized burst pulse samples, rather than digitized IF samples, on its fiber downlink. The exact placement and width of the burst window will depend on the trigger timing and digital filter specifications that the user has chosen, usually via the **Pb** and **Ps** plotting setup commands.

Following the burst window is a fixed-length sequence of 25 serial data bits which convey information from the RVP7/Main processor. The first four data bits form a characteristic (0,1,1,0) marker pattern. The first zero in this pattern effectively marks the end of the variable length burst window, and the other three bits should be checked for added confidence that a valid bit sequence is being received. Table 2–10 defines the interpretation of the serial data bits.

Table 2–10: Bit Assignments for the IFD Coax Uplink

Bit(s)	Meaning
1–4	Marker Sequence (0,1,1,0). This fixed 4-bit sequence identifies the start of a valid data sequence following the variable-length burst window.
5–20	16-bit multi-purpose data word, MSB is transmitted first (See below)
21	Reset Request. This bit will be set in just one transmitted sequence whenever an RVP7/Main reset occurs.
22	If set, then interpret the 16-bit data word as 4-bits of command and 12-bits of data, rather than as a single 16-bit quantity (See below)
23–24	Diagnostic select bits. These are used by the RVP7/Main power-up diagnostic routines; they will both be zero during normal operation.
25	Green LED Request; 0=Off, 1=On. The state of this bit normally follows the "Fiber Detect" LED on the RVP7/Main board.

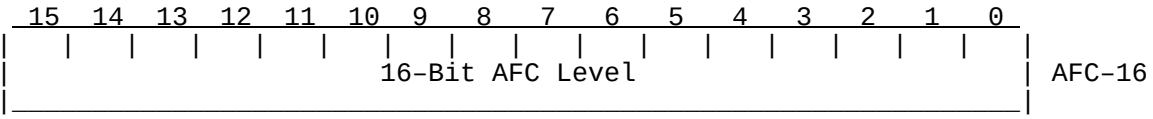
The period τ_s of the serial data is $(64/\ f_{aq})$, where f_{aq} is the acquisition clock frequency given in the **Mc** section of the RVP7 setup menu. For the default clock frequency of 35.975MHz, the period of the serial data will be 1.779µsec. The logic that is receiving the serial data should first locate the center of the first data bit at $(0.5 \times \tau_s)$ past the falling edge at the end of the burst window. Subsequent data bits are then sampled at uniform τ_s intervals.

The actual data sampling rate can be in error by as much as one part in 75 while still maintaining accurate reception. This is because the data sequence is only 25-bits long, and hence, the last data bit would still be sampled within $\pm$1/3 bit time of its center. Having this flexibility makes it easier to design the receiving logic. For example, if a 5MHz or 10MHz clock were available, then sampling at 1.8µsec intervals (1:85 error) would be fine. Likewise, one could sample at 1.75µsec based on a 4MHz or 8MHz clock (1:61 error), but only if the first sample were moved slightly ahead of center so that the sampling errors were equalized over the 25-bit span.

Interpreting the Serial 16-bit Data Word

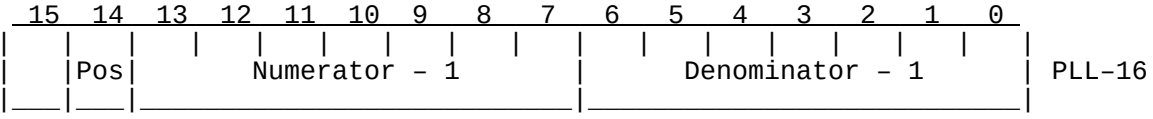
The serial 16-bit data word has several different interpretations according to how the RVP7 has been configured, and whether Bit #22 of the uplink stream is set or clear. The evolution of these different formats has been in response to new features being added to the IFD (Section 2.1), and the production of the DAFC Digital AFC Module (Section 2.4).

The original use of the uplink data word was simply to convey a 16-bit AFC level, generally for use with a magnetron system. Bit #22 is clear in this case, and the word is interpreted as a linear signed binary value. The use of this format is discouraged for new hardware designs, but it will always remain available to guarantee compatibility with older equipment.



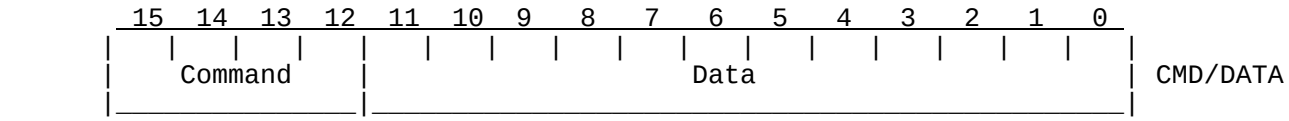
Level 0111111111111111 (most positive AFC voltage)
0000000000000000 (center AFC voltage)
1000000000000000 (most negative AFC voltage)

When the IFD is jumpered for phase locking to an external reference clock, then Bit #22 will be clear and the data word conveys the PLL clock ratio, and the Positive/Negative deviation sign of the Voltage Controlled Crystal Oscillator (VCXO). This format is commonly used with klystron systems, especially when the RVP7 is locking to an external trigger.



Note that the AFC-16 and PLL-16 formats can never be interleaved for use at the same time, since there would be no way to distinguish them at the receiving end.

Finally, an expanded format has been defined to handle all future requirements of the serial uplink. Bit #22 is set in this case, and the data word is interpreted as a 4-bit command and 12-bit data value. A total of *16x12=192* auxiliary data bits thus become available via sequential transmission of one or more of these words. The CMD/DATA words can also be used along with *one* of the AFC-16 or PLL-16 formats, since Bit #22 marks them differently.



Commands #1, #2, and #3 control the 25 output pin levels of the DAFC board. These transmissions may be interspersed with the PLL-16 format in systems that require both clock locking and AFC, e.g., a dual-receiver magnetron system using a digitally synthesized COHO. Note that the entire 25-bits of pin information are transferred synchronously to the output pins only when CMD=3 is received. This assures that momentary invalid patterns will not be produced upon arrival of CMD=1 or CMD=2 when the output bits are changing.

CMD=1	Data<0>	DAFC output pin 25
	Data<6>	Fault Input is active high
	Data<11:7>	Which pin to use for Fault Input (0:None)
CMD=2	Data<11:0>	DAFC output pins 24 through 13
CMD=3	Data<11:0>	DAFC output pins 12 through 1

These three digital AFC pinmap commands are recommended as a replacement for the original AFC-16 format in all new hardware designs. If you only need 12-bits of linear AFC, then map the AFC range into the –2048 to +2047 numeric span, and select binary coding format (See Section 3.3.6); the 12-bit data with CMD=3 will then hold the required values. To get a full 16-bit value, use a –32768 to +32767 span and extract the full word from both CMD=2 and CMD=3. Of course, other combinations of bit formats and number of bits (up to 25) are also possible.

Command #4 is used to control some of the internal features of the IFD. Bits <4:0> configure the on-board noise generator so that it adds a selectable amount of dither power to the A/D converters. This noise is bandlimited using a 10-pole lowpass filter so that most of the energy is within the 150KHz to 900KHz band, with negligible residual power above 1.4MHz. Each of the five bits switch in additional noise power when they are set, with the upper bits making successively greater contributions. Bits <6:5> permit the IF-Input and Burst-Input signals to be reassigned on the fiber downlink.

CMD=4	Data<4:0>	Built-in noise generator level
	Data<6:5>	IF-Input and Burst-Input selection 00 : Normal 01 : Swap IF/Burst 10 : Burst Always 11 : IF Always

2.5.2 Using the (I,Q) Digital Data Stream

The (I,Q) data stream that is computed by the FIR filter chips is communicated in real time to all of the DSP chips on the RVP7/Main and RVP7/AUX boards via an 18-bit data bus and a single clock. The "IBD<17:0>" data bus and "IBDCLK" clock signals are sourced on the P3 96-pin DIN connector of the RVP7/Main board (See Table 2–6). These TTL signals are normally kept internal to the RVP7, but some users may have a need to tap into them directly, e.g., to feed a separate data processor with the demodulated "I" and "Q".

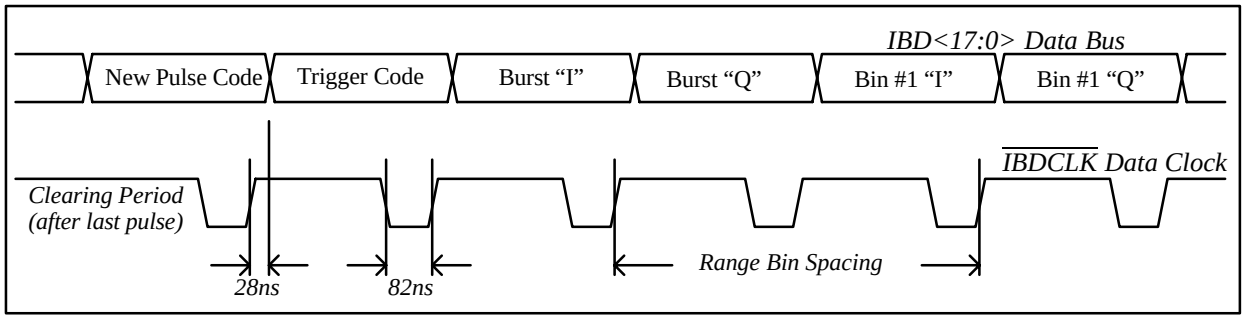
Making the electrical connections to the (I,Q) data stream is especially easy with the RxNet7 packaging of the RVP7, since the complete set of signals are driven onto a dedicated 68-pin connector on its backpanel. Moreover, special PECL drivers on that connector make it possible

to run the cable over distances as great as ten meters. Please see the *RxNet7 User's Manual* for full details, as this is the recommended approach for driving the (I,Q) data out to an external device.

If the RVP7's internal TTL signals are to be used directly, the physical connections must be made in such a way that no more than 12cm of additional wire length is added at the backplane. One way to do this would be to plug a custom driver board into an unused RVP7/AUX slot, from which the IBDxxx signals could be accessed. Another approach would be to mount the RVP7 board(s) in a completely custom backplane enclosure which also includes the user's equipment that receives the (I,Q) data stream.

The timing of the clock and data lines is shown in Figure 2–7 for the interval of time after the start of each transmitted pulse. The 18-bit data bus conveys two special code words at the beginning of each pulse, followed by (I,Q) for the Burst/COHO sample, followed by (I,Q) from the receiver. The receiver data continue to flow until the next transmitted pulse restarts the sequence anew, after a brief (approximately one range bin) clearing period. The data bus can be sampled on either the falling or rising edge of the clock, as there is an enforced 28ns data hold time after each rising clock edge. Using the rising clock edge will give the greatest data setup time, and this is usually preferred.

Figure 2–7: Timing diagram of the (I,Q) Data Stream



The "New Pulse" code is a unique 18-bit value that signifies the start of each new pulse of data. This is the only code or data word in which the MSB is zero.

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The "Trigger Code" follows immediately after the "New Pulse" code. It has a "1" in its MSB, and three different bit fields encoded into its low byte. These fields give information about the pulse itself. Codes that are not listed below are reserved, and will never appear on the data bus.

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	0	0	0	0	0	0	Flags		Bank			Waveform		

The 2-bit "Flags" field tells how this pulse will be used internally by the RVP7. This information is probably irrelevant to the external data processor, if all that it is doing is eavesdropping on the received data.

01 This is the final pulse of a collection of pulses that will contribute to the next processed ray.

The 3-bit "Bank" field tells the major classification of the pulse.

000 Normal pulse

001 Low PRF pulse during Dual-PRF mode

010 Blanked transmitter version of a normal pulse

111 Pulse used for receiver noise measurement (SNOISE Command)

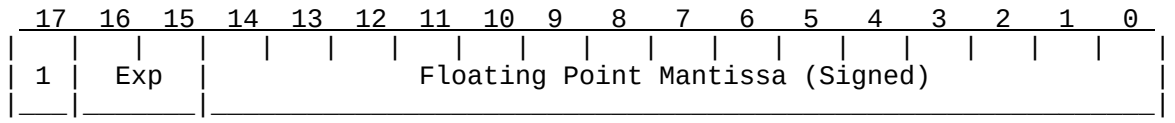
The 3-bit "Waveform" field indicates the minor classification of the pulse.

000 Normal pulse, or first pulse in a multi-part pulse sequence.

001 Indicates that this is an "alternate" pulse. This is the "V" channel for a single-channel polarization radar in which the receive or transmit polarization alternates pulse to pulse from "H" to "V". This is also the longer PRT pulse whenever DPRT (Dual-PRT) mode is running.

000-111 These incrementing codes will be output for the first eight pulses of any custom trigger pattern that the user has defined (See Section 6.14). If the custom pattern is more than eight pulses long, the "111" code will be held until the end of the sequence.

The (I,Q) data for the Burst/COHO sample, as well as for the receiver samples, all have the same floating point format consisting of a 2-bit unsigned exponent (*Exp*) and 15-bit signed mantissa (*Man*).



This format does not rely on a "hidden bit" in the mantissa. Rather, the mantissa is simply a 15-bit (generally unnormalized) value between –16384 and +16383, and the encoded floating point value is:

$$Value = Man \times 16^{Exp}$$

Note that the exponent shifts the value not in increments of one bit, but rather, by four bits (by factors of 16). The mantissa will always be the largest integer (i.e., greatest relative precision) that will fit into the fifteen available bits.

The overall dynamic range is 90dB while maintaining at least 66dB SNR within each sample. However, the format also gracefully underflows by allowing the mantissa to become small when *Exp=0*. This greatly extends the dynamic range into weak signals for which high relative precision is not required on each sample. The usable dynamic range of values over the entire receiver span is therefore approximately 125dB.